EXHIBIT A

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CASE: Grail v. Renesas
WITNESS: Donald Stern
DATE: 7/10/12

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Rachel F. Gard, CSR, RPR, CLR

*** U N C E R T I F I E D R O U G H D R A F T ***

clarify that. Of the selective power gating technology.

Q. And is all of the technology that you wanted to develop disclosed in the European patent?

MR. OPATKEN: Objection to form.

BY THE WITNESS:

A. I guess I don't understand the question. Can you ask that again?

Q. Sure. The European patent discloses certain technology, correct?

A. It discloses the selective power gating technology as it was in 1986, yes, or '88.

Q. So in 1997, was there anything in addition to the technology disclosed in the European patent application which you wanted to put into power gate?

A. I don't remember at the time.

Q. Is it reasonable to understand that there would be additional technology beyond what was disclosed in the European patent application that you wanted to put into power gate?

MR. OPATKEN: Objection to form.

A. I think there were probably some minor updates to the actual circuitry.

Q. So the business -- was the business plan to utilize technology that had already been disclosed in the European patent application to develop a new company?

MR. OPATKEN: Objection. Form.

BY THE WITNESS:

A. Yeah, that was part of it.

Q. And did you expect to be able to patent the technology disclosed in the European patent application, did you expect to be able to patent that in 1997?

A. I was looking at making some small improvements on the selective power gating technology.

Q. And what improvements were those?

A. Well, to update the circuitry and the chips that were used and the way that the circuit operated.

Q. Going back to Exhibit 54, who is bay owe, B E Y O?

MR. OPATKEN: Objection. Outside the scope of the deposition.

A. He was another investor that was interested in developing animation software.

Q. Did Mr. Bay owe ever have anything to do with the power gate technology?

A. No.

Q. And who is Werthime W E R T H I M E?

MR. OPATKEN: Objection. Outside the scope of the deposition.

BY THE WITNESS:

prototyping and patent filing on GSC 0000709?

A. Yes, I see that.

Q. And is that work that you would have done?

A. If I was going to do anything, yes, that would have been work that I would have done.

Q. So did you do that? Did you do circuit characterization in preparation for wafer prototyping and patent filing?

MR. OPATKEN: Objection. Outside the scope of the deposition.

BY THE WITNESS:

A. No, I did not.

Q. Did you do any work in relation to developing the Powergate technology?

A. No. In this time frame, no.

Q. In any time frame after 19 -- after the date of the Powergate agreement, July of 1997?

A. Did I do any work on the technology? No, I did not work on the technology.

MR. SWITZER: Why don't we take a break. 5 minutes, is that okay, counsel?

MR. OPATKEN: Sounds good.

THE VIDEOGRAPHER: We are going off the record at 11:08 a.m.

THE VIDEOGRAPHER: We are now going back on the

MR. OPATKEN: Objection. Calls for a legal conclusion.

A. Again, not being a lawyer, a breach I guess is the legal term. It was never executed upon.

None of the conditions in the agreement were ever met.

Q. And the conditions you're referring to, can you please list those for me that you consider not to have been met?

A. Well, incorporation of the company within 21 days of signing the agreement. It was not done.

Registering of the capital shares was never done.

Shares to be issued in the company was never done.

The nomination of directors was never done.

There was never a board meeting, so there was never a direct -- board of directors that was created. There was never any articles of associations or bylaws that were generated. There was never a convening of the board of directors.

There was never a resolution by the board.

There were never any votes.

The company Axon, or Powergate Limited was never created.

As far as I know, the money that was indicated that was going to be invested or loaned

was never done. It specifies it was supposed to be

done within 7 working days. That was never done. None of the options to purchase anything were ever exercised or done.

None of the employment agreements were ever drafted. There were never any votes or call to votes or any actions performed by shareholders or the directors. There were never shares transferred to anybody.

There were never any nondisclosure agreements signed.

There was never any technology developed for the company or in the name of the company.

It states there was supposed to be employment agreements within 30 days. That was never done.

And the parties on the other side were not loyal and honest to each other in that they agreed to do all of this in this agreement and they did not perform anything.

Q. And what is your basis for each of those allegations? Are there any documents that support that?

MR. OPATKEN: Objection.

BY THE WITNESS:

A. I don't remember exactly what that was in reference to.

Q. Do you see that second paragraph where it states: As I mentioned in my response to your questions, we need a copy of the nondisclosure agreement signed by the person/s who generated the questions in order to protect the technology.

Do you understand what that's referring to?

A. Yes, that was just a general procedure that anybody we talked to or was involved in any technology would sign a nondisclosure agreement.

Q. Those questions, was that referring to questions about the Powergate technology?

A. I believe it was the questions that we just reviewed in one of the prior exhibits which references the selective Powergate technology.

MR. SWITZER: No further questions on a

personal basis at this time.

MR. OPATKEN: All right. Well, unless there's any objections, I can just go ahead and start in with some questions for Mr. Stern.

Q. Mr. Stern, I just want to go back through some of these exhibits that Renesas' counsel has shown you. If you can look back at Exhibit 52, please.

A. Okay.

Q. This was your resume; is that correct?
A. Yes, I believe that's correct.
Q. And counsel for Renesas had you review from 1984 through 2000 -- I apologize, through about 2000. Either way, when you looked at this, is this a pretty accurate reflection of your employment history?
A. Yes, I believe it is.
Q. And can you show me where in this document you indicate your employment with Powergate Limited?
A. I don't indicate because I was never employed by Powergate Limited.
Q. So nowhere into your resume is there any indication that you were employed by Powergate Limited?

A. That's correct.
Q. And if you look around the time frame of 1997, specifically there's no reference of Powergate?
A. That's correct.
Q. And 1998, no reference of Powergate?
A. That's correct.
Q. And why is that?
A. Because I was never employed by Powergate Limited.
MR. SWITZER: Objection. Calls for a legal conclusion.

MR. OPATKEN:

Q. And if you can look back at Exhibit 55 for me --

A. Okay.

MR. SWITZER: One second counselor. All right.

Q. Looking back at Exhibit 55, can you tell me what is meant by first capitalization, second capitalization, and third capitalization in the numbered paragraphs?

A. I would assume that Robert was talking about incremental investments in the company.

Q. And to the best of your knowledge, was

there ever a first capitalization of $100,000 for Powergate limited?

A. No, not that I'm aware of.

Q. To the best of your knowledge was there ever a second capitalization for $200,000 for Powergate limited?

A. No.

Q. To the best of your knowledge, was there ever a third capitalization of $500,000 for Powergate limited?

A. No, there wasn't.

Q. What capitalization of Powergate limited are you aware of?

A. I'm not aware of any investment in the company.

Q. If you could do me a favor and look back at Exhibit 61, please?

A. Okay.

Q. I'm sorry. For the record, this is GSRE 348. I apologize. 347 through 349.

If you can turn to the second page, did you draft this document?

MR. SWITZER: Objection. Asked and answered.

BY THE WITNESS:

A. No, I don't believe I did.

Q. Do you know if this document was sent?

A. I don't know if it was sent. I don't believe that it was.

Q. If something were to be sent to the board of directors of Powergate limited, where would it go to?

A. I have no idea where it would go to.

Q. Why would you not know where it would go to?

A. Because there is no Powergate limited. If it was to go to anybody, I guess it would go to the list of people that are in the document.

Q. So is there any board of directors of which you're aware?

A. No, there's never been a board of directors of Powergate Limited, as far as I'm concerned.

Q. I'd like if you could to take a look back

at Exhibit 63. If you could turn to the second page, it's GSC 702.

A. Okay.

Q. What is this? What does it appear to be to you?

A. It appears to be an invoice.

Q. What is an invoice?

A. It would be a request for money to be paid.

Q. Does this indicate that money was paid?

A. Not to me, no.

Q. Is there any indication anywhere on this document that money had been paid by Powergate limited to you or anybody else?

A. No.

Q. So when we look here, what is meant by $4,000 due F/consulting fees? Perhaps let me take a step back and strike that.

Did you draft this invoice?

A. No, I didn't.

Q. Do you know who did draft this invoice?

A. I believe Robert drafted the invoice.

Q. Can you personally speak to the veracity of anything inside this invoice?

A. No, I cannot.

Q. So what would -- based on your understanding of this document, what would $4,000 due F/consulting fees mean, if anything?

ever sent, transferred or that any action was taken on this.

Q. Is it clear when or if this invoice was actually submitted to Powergate limited?

A. Well, it has an invoice date on it. But whether it was submitted, there's no indications. There's no emails or fax headers or any writing on it that it was sent.

Q. And the same, I guess, with the previous invoice you looked at; was there any indication there of a date of actual sending if, in fact, the invoice was ever sent?

A. No, there's no writings or any other documents. Typically if I had sent a fax, I would have signed and dated it that it was sent.

Q. If you can turn real quick to Exhibit 66 --

A. Okay.

Q. Again, is this just another invoice?

A. Yes, just another invoice.

Q. And any indication that this invoice was ever sent?

A. Nothing that's marked on it that indicates it was ever sent.

Q. Any indication that it was ever paid?
A. Nothing indicates that it was ever paid.
Q. Assuming for a moment that this had been sent, why would an invoice for May still have consulting fees from April? Would that be perhaps be because payment had not been made?
A. I would be guessing, but I would guess that that would be the case. It's dated May, that it would be indications that either the work had been done or the work was going to be done. I don't know. Again, I would be guessing, so I'm not going to guess.
Q. Rather than have you guess, let's talk about what you know personally.
To the best of your knowledge, the best of your recollection, did you ever receive payment for anything done for Powergate Limited?
A. Not that I'm aware of. I have no records and documents.
Q. If you turn to Exhibit 67, it's a single page GSC 675.
A. Yes, I have that.
Q. Did you draft this document?
MR. SWITZER: Objection. Asked and answered.

BY THE WITNESS:
A. I don't believe I did.

Q. And do you know who would have drafted this document?
A. I would assume that Robert had done it, but I have no confirmation, no way of confirming that.
Q. And it says at the top of the table: Don's salary.
A. Yes, I see that.
Q. And at the very top of the table it says Powergate?
A. Yes, I see that.
Q. Did you ever receive a salary from Powergate?
A. No, I did not.
Q. Did you ever negotiate which salary with Powergate?
A. No.
Q. If we look down below, in that first column it says paid by Moshe?
A. I see that.
Q. And in the very first column to the right there it says $10,000?
A. Yes.

Q. And if you look above it says in the first column, travel and E X P, July 10,000. Do you see that?
A. Yes, I see that.
Q. What is E X P, do you know?

A. I don't know the reason why it would have a date different from the top and the bottom unless the program that produced it dated it when it printed it.

Q. Are you typically in the habit of signing your documents by hand unless it's electronic communication?

A. Yes. I would sign a document if it was a fax or a letter, and typically if it was a fax when it was sent, I would initial and date it so that I know that it in fact had been faxed when it was put into the record.

Q. You can turn to Exhibit 74. This is GSC 720 through 723. When you state here on the first page Powergate does not require power to retain the data, is that referring to selective powergating?

A. Yes, it is.

Q. And how does selective powergating work?

A. The theory behind selective powergating is to store the data in a nonvolatile memory device, like a flash device, and then when the array or group of addresses is selected, to read the data out of flash into an SRAM type of a device so the computer can then access it and read and write the areas. And then once it's been Dee selected to restore the data back into a flash-like device.

Q. Now, is it just a coincidence that

Powergate limited has the name it has?

A. No, it's not a coincidence. It's reflective of the technology which is to selective PowerGate, or to turn on the sections that you're going to power.

Q. If you can go onto the third page, which is GSC 722 --

A. Okay.

Q. I believe question 4 and just below that is an answer. It says delaying the project is a sear use concern. The funding for this project has been delayed for several months. Do you see that?

A. Yes, I do.

Q. Do you know what that might be referring to?

A. I would assume that it was talking about that we had an agreement for doing Powergate and that it had not been funded.

Q. Now, whether -- if you think back to the Powergate agreement, it's Exhibit 57, you declared that you were in the possession of core technology and that you have knowledge and skills necessary experience for the development of the technology.

A. Yes.

Q. Having that knowledge and experience, can

you use that in any beneficial way without funding?
A. No, you need funding to design, build, manufacturing, market, and patent technology.
Q. So what can you do without any funding from Powergate Limited?
A. Come up with concepts and record them on a piece of paper.
Q. Let's look down a few paragraphs. It starts answer: Powergate is not developing any other products. What do you mean by -- what is meant by any other products?
A. I'm sorry. Where is that?
Q. Sixth paragraph down?
A. Back in this?
Q. Oh, I'm sorry. Yes, back in Exhibit 74.
A. On which page?
Q. Third page.
A. Third page. It was --
Q. I'm sorry, go ahead.
A. It was just an answer to his question comparing Powergate cost and performance to other development. And the response is, Powergate is not developing any other products. So this is just replying to his question.

Q. So Powergate's only technology was the Powergate technology, selective powergating?

A. Yes, Powergate's technology was selective powergating.

Q. Powergate limited, was it doing anything, any other technology?

A. Well, the intention was to do selective powergating, but the company was never started, so ...

Q. If you turn to Page 4, second paragraph, no funding has been available to engage my attorney yet. Delays in funding for this project have caused serious concerns. Did I read that accurately?

A. That's what it says.

Q. Now, are you aware in your relationship with Powergate limited of them ever providing funding sufficient to engage an attorney for patent purposes?

A. No.

Q. In your experiences with Powergate limited, are you familiar with significant delays with the funding for the project?

A. Well, again the project was never funded.

Q. Further below, the continued delay of

funds has prevented us from filing the patent?

A. Yes, that's what it says.

Q. And what is the date of this document to

the best you can ascertain?

A. 5/11/98.

Q. And so in 1998, was there a desire to file a patent relating to selective powergating technology or an improvement thereof?

A. Yes.

Q. And was any patent able to be filed relating to that technology?

A. No.

Q. And why not?

A. Because there was no funding to do so.

Q. Going back to Exhibit 75, which is GSC 728 --

A. Okay.

Q. -- you state in the fifth -- I'm sorry. Is that your signature on the bottom of the page?

A. Yes, that is.

Q. So you state on the fifth --

A. I'm sorry.

Q. Fifth paragraph, you and your father indicated that you would provide the involvement for

this project. And that's to Dudi or David Werthime; is that correct?

A. That's correct.

Q. And then further it states: All of your questions have been promptly answered. Is that accurate?

A. No, I'm not.

MR. OPATKEN: Perhaps we can take a quick break, reconvene and --

MR. SWITZER: I have a couple of questions to follow up on yours.

MR. OPATKEN: Oh, I'm not done yet.

MR. SWITZER: Okay. Fair enough.

THE VIDEOGRAPHER: We are going off the record at 3:00 p.m.

THE VIDEOGRAPHER: We are now going back on the record at 3:15 p.m.

BY MR. OPATKEN:

Q. Mr. Stern, I'd like you to take a look back at Exhibit 57. This is GSC 2949.

A. Okay.

Q. Just real quick, what is this document?

A. It's the agreement for developing selective powergating technology.

Q. So this is the reason why I guess we're here today, is this Powergate agreement.

A. Is that a question?

Q. It was more of a statement.

A. Okay.

Q. Who is this agreement between?

A. Robert Stern, myself, and Axon technology.

Q. I'd like to look here there's some whereas clauses on this first page. If you can look at the

third whereas clause, it states here: Don and Schneor wish to incorporate a company hereinafter the company, which will engage in the development of new architecture of electronic devices, hereinafter the products. Did I read that accurately?

A. Yes.

Q. And the Don referred to there, that's you?

A. That's correct.

Q. And the company, is that supposed to be Powergate Limited?

A. As I understand it, yes.

Q. And engage in development of new architecture of electronic devices, the products, what does the products encompass?

A. It encompasses what is described in the appendix as selective powergating.

Q. Now, did Powergate Limited, to the best of your knowledge ever manufacture any products?

A. No.

Q. To the best of your knowledge, did Powergate ever sell any products?

A. Powergate limited, no.

Q. Did Powergate limited ever design any products?

A. No.

Q. If we look below two more whereas clauses, it states that Don declares that he is in the

possession of the core technology necessary for the development of the products. Did I read that accurately?

A. Yes.
Q. And again is that Don, you?
A. That's correct.
Q. What was the date of this agreement?
A. June 30th, 1997.
Q. I'm sorry, is it July 30th, 1997?
A. Sorry, yes. July 30th.
Q. On July 30th of 1997, what technology was in your possession?
A. The selective powergating.
Q. On July 30th of 1997, were you in the possession of any technology related to inductive storage capacitants?
MR. SWITZER: Objection. Outside the scope.
A. No.
Q. On July 30th, 1997, were you in the possession of the '552 patent at issue in this lawsuit?
MR. SWITZER: Objection. Outside the scope as I understood it and as was instructed not to ask earlier, but please proceed.
Q. Well, just to be clear, the scope is the effect of the Powergate agreement on the ownership of the patent-in-suit?

MR. SWITZER: So questions of when he was in possession of the technology of the 552, which would appear to relate to conception or induction of practices that you vociferously argued we should not be able to inquire as to that.

MR. OPATKEN: I agree that there should be no inquiry into conception or induction of practice. But as to whether or not Mr. Stern was in possession of the core technology in the whereas clause of the Powergate agreement, if core technology could possibly relate to the '552 patent, it is within the scope.

Q. So July 30th, 1997, were you in possession of the technology embodied in United States Patent 6,642,552?

A. No.

Q. And what was the technology you were in possession of?

A. The selective powergating technology in '97.

Q. And is this agreement anywhere indicate that that was the technology that you were in possession of?

A. Yes. In the appendix it states that.

Q. And does this agreement anywhere indicate the existence of or your possession of technology relating to U.S. Patent 6,642,552?

A. No.

Q. And if you look at the next whereas clause, it states: The development of the products necessitates at the first stage a substantial financial investment. Did I read that accurately?

A. Yes.

Q. To the best of your knowledge, was there ever a substantial financial investment?

A. No.

Q. And was Powergate limited ever able to develop the products relating to selective powergating as contemplated by this agreement?

A. No.

Q. And why was PowerGate limited not able to develop products?

A. Because it had no funding.

Q. If we turn to the next page, GSC 2950, Paragraph 2 B, which states: Within 21 days from the date of signing this agreement, the parties will sign the memorandum of association and the articles of association. Did I read that accurately?

A. Yes.

Q. Did you ever draft a memorandum of

Q. And to the best of your knowledge, did Axon or any persona affiliated with Axon ever sign a memorandum of association?

A. Not that I'm aware of.

Q. Did they ever sign, to your knowledge, a memorandum of association within 21 days of July 30th, 1997?

A. Not that I'm aware of.

Q. And is Axon a party to this agreement?

A. Yes, they are.

Q. It continues, the articles of association, did you ever draft articles of association?

A. No.

Q. Have you ever seen articles of association?

A. No.

Q. Are you aware of the existence of articles of association?

A. No, I am not.

Q. Did you ever sign articles of association?

A. Having to do with Powergate Limited, no.

Q. And are you a party -- well, and you're a party to this agreement?

A. Yes, I am.

Q. And to the best of your knowledge, did Bob Stern ever sign articles of association?

A. Best of my knowledge, no, he never did.

Q. To the best of your knowledge, did Axon or anyone affiliated with Axon ever sign articles of association?

A. Not that I know of.

Q. If we move down below to Paragraph 3-A, it states: The registered capital of the company will be I S 30,100 divided to 30,000 ordinary shares of one shekel, nominal value each and 100 management shares of one shekel nominal value each.

To the best of your knowledge, was there ever any registered capital of Powergate limited?

A. Not that I'm aware of.

Q. Paragraph 3-B, the issued share capital of the company will be 4 management shares and 944 ordinary shares to be held by the parties as follows. Did I read that accurately?

A. Yes.

Q. To the best of your knowledge, were there ever any issued shared capital?

A. Not that I know of.

Q. It states below: Don colon 1 management share and 300 ordinary shares. Did I read that accurately?

A. Yes.

Q. Did you ever receive 1 management share of Powergate limited?

A. No.

Q. Did you ever receive 301 ordinary shares of Powergate Limited?
A. No.
Q. Did you ever receive any shares of Powergate Limited?
A. No.
Q. To the best of your knowledge, did Robert Stern ever receive any shares of Powergate limited?
A. No.
Q. To the best of your knowledge, did Axon ever receive any shares of Powergate limited?
A. Not that I know of.
Q. Have you ever returned any shares to

Powergate Limited?
A. No.
Q. So assuming, despite your statements to the contrary that you had received shares, if you ever received such shares, you would still have 301 ordinary shares and 1 management share?
A. If any shares had been issued, yes, I guess I would still have them.
Q. And Bob would still be in possession of 301 ordinary shares and 1 management shares, if he had ever received any?
A. As I understand it, that would be correct.
Q. If you could please turn to the following page, GSC 2951, Paragraph 5, entitled rolls of the

parties, and it states that Axon is entering into this agreement and is ready to grant loans to the company as mentioned hereafter, mainly because of, and this is Schneor and Don because they are shareholders in the company. Do you see this, Paragraph 5?

A. Yes.

MR. SWITZER: Objection. Misstates the document.

Q. I can read the entire paragraph just to

keep the record clear. The entirety of Paragraph 5 reads: Schneor and Don declared that they know that Axon is entering into this agreement and is ready to grant loans to the company as mentioned hereafter mainly because of their declaration that each of them has the knowledge and special skills in their field and because they are shareholders in the company and will work in the company for at least 2 years using this knowledge and skills and best efforts for the purposes of developing the products for the company.

Is that an accurate reflection of Paragraph 5 of the Powergate agreement?

A. Yes.

Q. And it states here: Because they're shareholders in the company. Are you or were you ever a shareholder in the company?

occurred and there were never any loan documents drawn up stating the terms of the loan.

Q. And if you look at subsection B, it states: The shareholders loan will be spread into

several payments in sums and dates according to the company needs and the decisions of the board of directors.

A. I'm sorry. Which paragraph?

Q. I'm sorry, continuing onto the next page, GSC 2952 --

A. Okay. And which --

Q. Subsection B?

A. Okay.

Q. States the shareholders loan will be spread into several payments in sums and dates according to the company's needs and the decisions of the board of directors from time to time and according to the company's business plan, appendix A. Did I read that accurately?

A. Yes.

Q. To your knowledge was there ever a board of directors?

A. No.

Q. Was there ever decision us of a board of directors?

A. No.

Q. Were there ever loan payments in smaller

24 amounts less than $100,000 to the best of your

1 knowledge?
2 A. No.
3 Q. And when it states here in the last
4 phrase, according to the fundamental business plan,
5 appendix A, what is meant by fundamental business
6 plan?
7 A. The document in appendix A that describes
8 the intention to develop and market selective
9 powergating.
10 Q. So when you entered into this agreement on
11 July 30th of 1997, it was your intention to develop
12 selective powergating technology?
13 MR. SWITZER: Objection. Leading.
14 Q. Is that correct?
15 A. That's correct.
16 Q. Is it your understanding also that any
17 loans would be to develop that same technology?
18 A. Yes, that's correct.
19 Q. If you could turn to what's labeled GSC
20 2954 --
21 A. Okay.
22 Q. And you were asked earlier about
23 Paragraph 12, I believe. It states: Field of
24 activity of the company. What is the field of

activity of Powergate limited?

A. As I understand it, the field of activity is the development of selective Powergate technology.

Q. Is there anything in this agreement that supports your understanding?

A. The Appendix A, which describes the technology as selective powergating.

Q. And if we look at the second paragraph of Section 12, it states: Each party undertakes to sign any document necessary for the implementation of the above.

Did I read that accurately?

A. Yes.

Q. To the best of your knowledge, did you ever sign any document necessary to transfer any technology to Powergate limited?

A. No, there were never any documents signed for Powergate limited.

Q. To the best of your knowledge, did Bob Stern ever sign any documents necessary to transfer any technology to Powergate limited?

A. As far as I know, no, there was nothing signed.

Q. And to the best of your knowledge, did Axon ever take any steps to sign any documentation necessary for the transfer of technology to Powergate limited?

A. As far as I know, they've signed nothing.

Q. You stated earlier in your prior testimony that pre agreement technology was not to be included in the Powergate agreement; is that correct?

A. That's what I understood.

Q. But is it also your understanding that improvements upon pre-existing technology may have been subject to the Powergate limited agreement?

A. I guess that could be interpreted that way. I don't really understand from a legal point of view.

Q. I guess, for example, the selective powergating technology had been in development for a number of years, correct?

A. Correct.

Q. And was it your understanding that there were further developments that could be done with selective powergating technology?

MR. SWITZER: Objection. Leading.

A. I had some concepts that I wanted to

further develop, and I was looking for funding to pay for that development. And if it led to something good, then patent protection.

Q. And so during the execution of the Powergate agreement, was it contemplated that further developments in selective Powergate technology may be transferred to Powergate limited?

MR. SWITZER: Objection. Leading.

BY THE WITNESS:

A. Yes.

Q. If you look at Paragraph 13 -- actually, let me go back just one second.

Did you ever assign selective Powergate technology to Powergate Limited?

A. No.

Q. Did you ever transfer selective powergating technology to Powergate Limited?

A. No.

Q. Looking at Paragraph 13, titled employment agreements, it states: The parties will prepare the employment contract with Schneor and Don within 30 days. Those contracts will be considered as part of this agreement. Did I read that accurately?

A. Yes.

Q. Did you ever prepare an employment contract between yourself and Powergate Limited?

A. No.

Q. Did you ever prepare an employment contract between Bob Stern and Powergate limited?

A. No.

Q. Did Bob Stern ever prepare an employment contract between either yourself or himself and Powergate limited?

A. No, not that I'm aware of.

Q. And did Axon ever prepare any employment contract with either you or your -- or Bob Stern?

A. They never produced anything, no.

Q. Are you aware of them even preparing an employment contract with yourself or Bob Stern?

A. They were supposed to, but they never did.

Q. So within 30 days, are you aware of the existence of any employment contract between yourself or Bob Stern and Powergate limited?

A. No.

Q. To this day, have you ever seen any employment contract with anybody in Powergate limited?

A. Nothing.

Q. But these contracts were supposed to be considered as part of this agreement; is that correct?

A. That's correct.

Q. And they were supposed to be prepared within 30 days; is that correct?

A. That's correct.

Q. I'd like to turn now to the following page, GSC 2955. Is this the appendix to which

you've been referring thus far?

A. Yes.

Q. At the very top it says Powergate, Inc. Do you know why it says Powergate, Inc.?

MR. SWITZER: Objection. Asked and answered.

A. No, I assume that's the name that Robert Stern is using to represent the technology.

Q. And what was the date of this document?

A. According to what it says, June 30th, 1997.

Q. And do you know what the purpose of this document was when it was -- I'm sorry.

Date of composition, does that subject to you this document was created on June 30th, 1997?

A. That the document was created before or updated or that's the current date on the document

as it is today.

Q. And do you know what the purpose of creating this document would have been?

A. Was to describe the selective powergating technology so that we could enter into an investment deal.

Q. And we see below Powergate Inc. it says advancements in selective Powergate for energy reduction and heat re deduction. Did I read that accurately?

A. Yes.

Q. And I remember we looked back at

Paragraph 6 B. The agreement considers this a fundamental business plan, correct?

A. Yes, that's what it says.

Q. So what is your understanding of the scope of technology even being contemplated by the parties to the Powergate Limited agreement?

A. The scope is for advancements in selective powergating.

Q. Now, does selective powergating include nonvolatile memory devices?

A. That's part of the operation of the device, yes.

Q. So what is the relationship between selective powergating technology and nonvolatile memory devices?

A. As part of the operation of the device, when the device is powered up, it was supposed to read out of a flash-like or an EEPROM nonvolatile memory device into an SRAM so the computer could then access the SRAM to get high-speed access to the data.

Q. Is SRAM nonvolatile?

A. SRAM is volatile.

Q. So am I understanding correctly, the idea between selective powergating was switching between volatile and nonvolatile memory?

A. In a nutshell, yes.

Q. And again, you didn't create this document, this appendix A, did you?

A. No, it was Robert Stern that produced this document.

Q. Now, if we can turn to the following page, GSC 2956, and if we look down at the third paragraph from the bottom, which starts whether it is called, and the last sentence, the sentence reads intrinsic to the memory's architecture is the Powergate's

logic to keep the circuits turned off when they do not have to be specifically turned onto operate a program or perform a read/write. Did I read that accurately?

A. Yes.

Q. What is that describing?

A. It has to do with the powergating or the turning on of logic as the computer is accessing it.

Q. And this is selective powergating?

A. This is selective powergating.

Q. And if we turn to the next page, GSC 2957, the very last paragraph, this, by the way, the heading is a history of prior technologies. These prior paragraphs, the first few paragraphs, do they discuss prior technologies?

A. Yes, they do.

Q. And if we look at this last paragraph, it states: In common practice, the whole memory unit

is powered to operating current for access, and then the whole unit is powered down. It is a major point of this invention to maintain a whole memory unit in an off state and through selective powergating to supply operating power for the particular memory elements being accessed and only for the time

necessary for them to be accessed thereby achieving a savings in energy and reduction of heat sufficient to allow for dense packing and vertical layering of memory circuits.

Did I read that accurately?

A. Yes.

Q. And what is this paragraph discussing?

A. The use of selective powergating to power on and off certain areas of memory.

Q. Again, it is a major point of this invention, what is this invention?

A. The invention of selective powergating.

Q. So was it your understanding that the agreement with Powergate limited would be limited to this intention, namely the selective powergating technology?

A. Yes.

Q. And if we turn to the following page, GSC 2958, in the fourth paragraph, on the pages entitled embodiments of the technology, the fourth paragraph, first phrase states: Selective gating of power can

also be implemented as a means of reducing power consumption and heat generation in computer systems.

Is that an accurate reading?

A. Yes.

Q. And is that again talking about selective powergating, the technology?

A. Yes.

Q. And if we look at the last sentence of the same paragraph: Selective gating of power can be used in robot Android-type devices to provide operating power to a specific electronic function only when that specific function is to be performed and turn off the operating power to that function or the placing of that function into a lower energy wait state or standby state when it is not being performed. Did I read that accurately?

A. Yes.

Q. And again, what is this sentence discussing?

A. The discussing of the use of selective powergating and how it would operate.

Q. So after reviewing this Powergate agreement and appendix A, what was contemplated by you in entering this agreement?

A. For the development, production, and marketing of selective powergating.

Q. And what did you bring to the table?

A. The selective powergating technology.
Q. And what was Axon going to bring to the table?
A. The investment to bring the technology forward.
Q. And did Axon ever provide money to develop selective powergating technology?
A. No, they didn't.
Q. Now, could you fully perform your obligations under the Powergate agreement without funding?
A. No.
Q. When you initially didn't receive funding, did you just stop; or did you take further efforts to obtain funding or to convince Axon to perform its obligations under the agreement?
A. Well, we looked for alternate sources of funding.
Q. Just with Axon?
A. With Axon, with Axon we kept going back because they kept expressing an interest that they were interested in working with us to develop the technology, but they never did anything. They just kept expressing interest and asking questions.

Q. So do you believe any technology, including the selective powergating technology was ever transferred to Powergate limited?
A. No.
MR. OPATKEN: Where are we on exhibits?
MR. HAWKINS: We are at I believe 78. Yes.
Q. I'm going to hand you what's marked as 78. Do you recognize this document, Mr. Stern?
A. It's the inductive storage capacitive patent.
Q. What was the filing date of this patent?
A. It was filed on February 2nd, 2001.
Q. In 1997, or more specifically July 30th of 1997 when you entered into the Powergate agreement, did you possess the technology embodied in the 664 '552 patent?
A. No.
Q. Out of curiosity, take your time if you need to, does this '552 patent discuss selective powergating?
A. No, it does not.
Q. Does the technology of the '552 patent embody the technology of selective powergating?
A. No, it does not.

Q. If you could turn to column 16 of the '552 patent --

A. Okay.
Q. It begins about a third of the way down with the claims of a patent. If you could just review, for example, Claim 1. And please tell me if Claim 1 claims anything related to selective powergating?
MR. SWITZER: Objection to the extent you're calling for a legal conclusion.
BY THE WITNESS:
A. No, there's nothing, as I understand it, in Claim 1 that has anything to do with selective powergating.
Q. And again, why the name Powergate?
A. It had to do with turning on or gating power to an electronic or memory element.
Q. When we looked at the appendix in the multiple discussions of selective powergating, have you ever done any work with selective powergating? Have you ever -- strike that.
Have you ever filed a patent related to selective powergating?
A. Yes.

Q. If you can take a look at Exhibit 53.
A. Okay.
Q. Is this a European patent application?
A. Yes, it says European patent application on it.

Q. And what is the title of this European patent application?

A. Selective powergating.

Q. Is it your understanding this patent application encompasses technology generally relating to selective powergating?

A. Yes.

Q. Does anything, to the best of your knowledge in this patent discuss inductive capacitants or inductive storage capacitors?

A. No.

Q. And likewise, in the appendix of Exhibit 57, is there any mention or discussion of inductants, an inductor capacitor or any similar description of technology otherwise embodied in the '552 patent?

A. I'm sorry, Exhibit 57?

Q. Exhibit 57, the Powergate agreement?

A. Is there anything in 57 that talks about

inductive capacitants, is that the yes?

Q. Yes. Is there anything in Exhibit 57 of its appendix that discusses inductants, an inductive capacitor, or similar technology?

A. No.

Q. Is there any mention of the '552 patent?

A. No.

Q. To this day, have you ever once considered

yourself employed by Powergate limited?
A. No.
Q. Did you ever assign -- strike that.
Do you know if Powergate ever had any employment agreements?
A. Powergate limited never had an employment agreement.
Q. When was the last time you spoke with Moshe Cohen?
A. 10-plus years ago.
Q. What about Dudi Werthime?
A. The same or more.
Q. And what about anybody at all affiliated with Powergate Limited?
A. Same. More than 10, 10-plus years ago since the discussion came up.

Q. Has anyone affiliated with Powergate Limited ever stated that they have a claim to the '552 patent?
A. No.
Q. Is it safe to say that selective powergating and inductive capacitants are broadly two different means to a similar end?
MR. SWITZER: Objection. Leading.
MR. OPATKEN: Let me rephrase.
Q. In the semiconductor memory field, what is the goal? What is the future?

A. Faster, smaller, less power, less cost.
Q. Is selective powergating a way to potentially achieve any of those goals?
A. Yes.
Q. And likewise, while a different technology, is inductive capacitants another way to potentially achieve those goals?
A. Yes.
MR. OPATKEN: You'll have to forgive me I forgot the exhibit again.
MR. HAWKINS: 79.
Q. I'm going to hand you what's been marked as Exhibit 79?

MR. SWITZER: Objection. This document appears to be outside the scope. But please feel free to continue.
Q. Do you recognize this document, Mr. Stern?
A. Yes, I do.
Q. And what is this document?
A. The sale and assignment of the inductive storage capacitive technology to N V memory.
Q. And this is a written assignment of the inductive storage capacitants technology to N V memory?
A. Yes.
Q. I'm going to hand you what's marked as Exhibit 80?

A. That's what it appears to be, yes.
Q. And it's an assignment from you to Grail Semiconductor, correct?
A. It says that I've assigned the patent to Grail Semiconductor, yes.
Q. It doesn't say that it was assigned to Powergate Limited, correct?

A. Correct.
Q. I'm going to hand you what's marked as Exhibit 81. Do you recognize this document?
A. It appears to be a query into the United States Patent and Trademark Office.
Q. What is the query for?
A. Powergate Limited, to see what has been assigned to them.
Q. And this is the first page, so the first page is a search for Powergate limited as an assignee; is that correct?
A. It's search for Powergate limited, yes.
Q. LTD?
A. LTD.
Q. And were there any results to that search?
A. None.
Q. And if you look to the next page, what does this page reflect?
A. It's a search of assignees for Powergate limited with no data available.

Q. So having reviewed all of this material, the Powergate Limited agreement, the appendix, all the other various documents, do you believe that you assigned anything ever to Powergate Limited?

A. No.

Q. Did you ever intend to assign anything to Powergate Limited?

A. Yes, when I signed the agreement with the Israelis.

Q. Did that intention come with conditions?

A. Yes.

Q. And were those conditions ever met?

A. No.

Q. Did you ever assign the '552 patent to Powergate Limited?

A. No.

Q. Did you ever assign inductive storage capacitor technology to Powergate Limited?

A. No.

Q. Did you ever sit down and discuss inductive storage, inductive capacitants with anyone affiliated with Powergate limited?

A. No.

Q. So as you sit here today, who do you think owns the '552 patent?

A. Grail Semiconductor.

Q. Is it possible that anybody else could own

24 the '552 patent in your opinion?

1 A. No.
2 MR. OPATKEN: I have no further questions.
3 MR. SWITZER: Okay. Can we take a 5 minute
4 break. Then I'll have some I guess follow-up
5 questions.
6 THE VIDEOGRAPHER: We are going off the record
7 at 4:07 p.m.
8 THE VIDEOGRAPHER: We are now going back on the
9 record at 4:19 p.m.
10 BY MR. SWITZER:
11 Q. Mr. Stern, could you please take a look
12 again at Exhibit No. 55, that's GSC 0000769.
13 A. Is it a one-page?
14 Q. A single page, yes, sir, on the top left
15 it states Wednesday, June 25th, 1997?
16 A. Okay. I have that.
17 Q. Do you recall counsel for Grail asked you
18 about the first capitalization, second
19 capitalization, and third capitalization that's
20 referenced on that document?
21 A. Yes.
22 Q. Let me first bring your attention, do you
23 see a date on the top left of Exhibit 55?
24 A. There's a date on the top, Wednesday,

Grail counsel's objections.

A. Yes.

MR. SWITZER: 5556929 --

MR. OPATKEN: It's not getting into the record. With all due respect, you are so far outside the scope of cross-examination at this point. It's not

going into the deposition record.

MR. SWITZER: I guess at this point, because counsel has instructed the witness not to answer any questions, we will hold it in abeyance, thank you.

MR. OPATKEN: I'd like to designate the entirety of the record as highly confidential, attorneys' eyes only.

MR. SWITZER: All right. So 10:00 a.m. tomorrow morning.

THE VIDEOGRAPHER: We are going off the record at 4:32 p.m.

EXHIBIT B

UNITED STATES DISTRICT COURT

FOR THE NORTHERN DISTRICT OF CALIFORNIA

SAN FRANCISCO

GRAIL SEMICONDUCTOR,	:	
Plaintiff,	:	Case No.
v.	:	3:11-CV-03847-JCS
RENESAS ELECTRONICS AMERICA, INC.,	:	
Defendant.	:	

CONFIDENTIAL

Videotaped Deposition of ROBERT STERN

Santa Barbara, California

Thursday, March 1, 2012

9:12 a.m.

Job No.: 17960

Pages: 1 - 249

Reported by: Kristin Vargas, CSR

the company. They would bring in, I think, a couple of million dollars. They agreed to bring in to go to the next step. 04:20:17 04:20:20 04:20:24

Q I would like to direct your attention to Paragraph 2B, which is on 2950. 04:20:48 04:20:50

A Uh-huh. 04:21:03

Q Did you ever sign a memorandum of association? 04:21:03 04:21:06

A I don't recall. It's possible. I don't recall. They were already in problems from the start because they did not incorporate the company within 21 days. And so from day one, we were, in my terms, hung out to dry. They just didn't give us the money on time. They didn't do anything they said they were going to do. 04:21:11 04:21:14 04:21:21 04:21:23 04:21:32 04:21:34 04:21:37

Q Did you sign any Articles of Incorporation? 04:21:44 04:21:49

A I don't recall. I don't have a copy of it so I don't remember. 04:21:50 04:21:52

Q I would like to direct your attention to Paragraph 3 on 2950. 04:21:53 04:22:08

A Okay. 04:22:24

Q Was this an accurate representation of the distribution of shares? 04:22:24 04:22:26

A I don't recall ever receiving any shares. 04:22:33

So I don't think there was ever any distribution of shares. I don't recall any distribution of shares. This was proposed distribution of shares. But I don't have anything in my records or recollection that I ever received any shares. 04:22:35 04:22:38 04:22:41 04:22:44 04:22:47

Q So do you think you -- you -- let's start with do you think you are a shareholder of Powergate based on this? 04:22:50 04:22:53 04:22:56

A I don't know Israeli law. It seems like after 15 years, if the company has been lying dormant, they didn't issue shares, they breached the contract, they refused to have shareholder meetings, they refused to have directors' meetings -- I don't know. This is a legal question. It's out of my scope. I don't know how to answer that. 04:23:03 04:23:06 04:23:09 04:23:12 04:23:15 04:23:18 04:23:20

Q Let's look at Paragraph 4 on 2950, Board of Directors of the company. 04:23:44 04:23:51

A I don't understand it. "Will expired" -- what does that mean? Okay. Okay. What is your question? 04:24:21 04:24:22 04:24:38

Q The question is we had discussed this earlier that you were on the Board of Directors for Powergate? 04:24:38 04:24:40 04:24:48

A I didn't know there was an actual election of board members, but yeah. I don't know if that's 04:24:50 04:24:52

STATE OF CALIFORNIA)
) ss.
COUNTY OF LOS ANGELES)

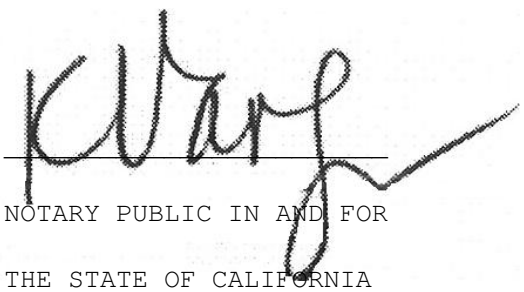
I, Kristin Vargas, Certified Shorthand Reporter, Certificate No. 11908 do hereby certify:

That prior to being examined, the witness named in the foregoing deposition was by me duly sworn to testify to the truth, the whole truth, and nothing but the truth;

That said deposition was taken down by me in shorthand at the time and place therein named and thereafter reduced to typewriting under my direction, and the same is a true, correct, and complete transcript of said proceedings;

I further certify that I am not interested in the event of the action.

Witness my hand this 3rd day of March, 2012.



NOTARY PUBLIC IN AND FOR
THE STATE OF CALIFORNIA

EXHIBIT C

Donald S. Stern
+1-408-406-3758

Objective: Development of new systems and architectures.

Summary:

Exceptionally strong background in executive management, mobile products, computers architecture, semiconductor processing, communications protocols and embedded control systems. Experienced in hardware, software, microcode, and communications architecture, design and development. Also proficient in user interfaces and teaching skills. Team building experience with project management focused on the timely completion and delivery of products to the market place.

Technology Developed:

- Architected, designed, patented and wrote a universal graphical programming language.
- Architected, designed, patented and wrote a universal operation system.
- Designed and wrote 3 new patents for new high effect Solar Panel and Hydrogen generator for production of Solar Farms
- Architected, designed, and wrote over 4 patents applications for new mobile data delivery capabilities for all mobile devices.
    - System includes Emergency Broadcast technologies for global implementation.
    - A new advertising delivery technology for Mobile devices.
    - 4 patents filed and nine provisional applications.
    - Developed a tunneling protocol for mobile devices.
- Designed and delivered a Mobile advertising system for real time push deliver system for internet content and advertising.
- Architected and designing new global system for communication between IP devices.
- Designed and developed real time, dynamic configurable Interactive Voice Response (IVR) system.
- Designed and developed Natural Language search interfaces for cellular phone data access.
- Designed an auto insert of Web information retrieval plug-ins for Chats and Blogs.
- Designed and developed an international SMS (PSMS) application and billing system.
- Designed and deployed tools set for a large (500 seat) real-time interactive support center.
- Conceived the theory for and patented a new solid-state semiconductor memory technology, and designed and developed a new architecture to replace Flash, DRAM and SRAM.

- Design architect for new IOS for Cisco Routers, which allows for online upgrades and new feature additions without rebooting.
- Developed classroom and Web based education E-Learning for Cisco systems.
- Designed and developed graphical user interface applications for interactive TV.
- Designed and developed Windows 3.1, 95, 98, NT4 and NT5 device drivers
- Developed new DVD standards for interactive multimedia (DVD Standard 0.9 and 1.0).
- Designed and developed standard for infrared communications for consumer electronics devices (IrDA).
- Designed and developed products for Sega, JVC, NTT, Intel and Microsoft.
- Developed drivers to automatically start a CD application when a CD is inserted into a PC and end the application when the CD is removed (Autoplay).
- Designed and developed serial, keyboard, USB infrared transmitters and receiver circuit, firmware and drivers for Windows 3.1, 95, 98, NT4, and NT5 for both unidirectional and bi-directional wireless keyboards, pointing devices, SmartCard, and paper-based remote controls.
- Designed, developed and manufactured 3D Joystick for Sega Saturn sold by Sega.
- Designed, developed and manufactured wireless paper-based remote control karaoke book for Japan sold by NTT.
- Development of hardware including circuit design, PCB layout and 8-bit microcontroller firmware to interface to Windows PC platform.
- Developed Internet server (IIS) application and Multimedia video layout tool and application.
- Design and development of a Windows-based CASE software product to Windows NT, converted software base from C to a C++ object-base system. Also added an open-ended API for the support of new communications protocols.
- Responsible for designing and prototyping of several semiconductor process modules.
- Developed and executed project plan for building prototype semiconductor wafer cleaning system.
- Developed a plan for manufacturing a semiconductor MESC module including a Bill of Materials with assembly, testing and operational documentation.
- Designed graphical control system user interface using distributed OOP's Windows-base system on QNX platform.
- Architecture and project manager for Concept II cluster tool.
- Chair of the SEMI/MESC control and communication task force.

- Implemented AI Expert-based system diagnostics system for diagnosing semiconductor tool failures.
- Responsible for Novellus Concept One Software and control system enhancements.
- Designed and installed an in-house LAN and MIS VAX / ASK system for accounting and manufacturing.
- Development products including the following protocol coax CUT, COAX DFT, BSC, ASC, SNA, LU6.2, SRPI, SSA, Routers, SNA Gateway, X.25 and LANs.
- Developed IBM Mainframe Host to PC software and hardware PC high-speed file transfer and virtual disk.
- Designed and implemented customer support incident tracking system.
- Installed a multi-IBM Mainframe host and PC data center with international dialup and network access.
- Designed and developed an OS/2 Communication Manager product.
- Designed and developed a PC-based FM single sideband mail service for ABC Corp. and Epson (Lotus signal).
- Developed the hardware, software and microcode (BIOS) for this real-time on-line service. System included central host computer with uplink to satellite, which injected the real-time data onto an FM station transmitter sideband carrier. Satellite downlink data was received by a PC and written to disk or printer. Designed hardware and software including low-level microcode interface and PC application.
- Provided consulting services to Amdahl customers through the Amdahl Product Support division.
- Developed VM conversion software tool package with VM and MVS software modifications.
- Developed, wrote, and presented classes on VM, MVS and 580 hardware from usage to internals.
- Developed a complete Video-training program including video pre- and post-production.
- Developed VM and MVS performance measurement tools.
- Project managed Amdahl's internally developed software tools for field support.
- Member of Amdahl 580 microcode, macrocode bring up team and design group for 580 VLSI packaging.
- Installed, maintained and tuned an on-line VM/MVS CICS host computer system for at insurance inquiry system.

Company Experience:

August 2008 to Present – MOM OS LLC, **Delaware**
Founder.

Patented, architected, designed and wrote a new universal graphical programming language and a new distributed open source operation system. Develop a web server using the new OS and language along with a new user application interface. Create over 15 new patents for data handling and graphical languages.

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May 2006 to July 2008 – **Global Mobile Technology, Singapore, Philippines, California**
Founder, Director, CTO, Chief System Architect.

Patented, architected, designed, managed and delivered a new cellular phone application that allows any cellular user to receive rich web and advertising content pushed real time to the screen of their phone. Built development center, hire complete staff and setup infrastructure to deliver new Internet Mobile software system. Meet with customers all over the world to setup new product deployment and wrote the product business plan and full project plan. Managed over 100 people including operations and engineering.

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July 2005 to April 2006 - **AskMeNow, Irvine, CA**
CTO

Architected, designed, and managed development team to build and deploy a new cellular phone application that allows any cellular user to ask any question and receive an answer within three minutes. Created a dynamically configurable Interactive Voice response (IVR) system that allows a phone user to have custom IVR menus. Created a natural language interface using both an SMS and a custom application interface to access Web data in real time. Built a 500 seat customer support center with a Web based interface in Asia to support large enterprise customers (ESPN, AVIS, Rogers wireless, and others).

Management experience: Defined positions, hired and managed three teams of developers (Ohio, Manila, Calif.) and support engineers (Manila). Defined, created and maintained a company wide and third party incident tracking system. Built and managed a complete product development and deployment plan which was presented and approved to top management and provided weekly status for executive staff.

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February 2000 to July 2005 – **Grail Semiconductor, San Jose, CA,**
Grail Technology, Singapore
Founder, Director, CEO, President, Architect

Conceived the theory for a new solid state semiconductor memory technology. Designed, developed, patented a new non-volatile solid state semiconductor memory technology intended to enhance and

combine the functions and best attributes of SRAM, DRAM, and FLASH into one non-volatile semiconductor memory device.

Management experience: Setup Corporation in California and Singapore. Wrote business plan, created five year budget and marketing plan. Setup semiconductor development lab, offices and hired staff. Worked with corporation attorneys and patent attorneys. Created and presented presentation for raising over one million in capitol.

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November 1998 to February 2000 - **Cisco System, Inc., San Jose, CA**
IOS Architecture, Educational Specialist

Developed classroom and Web based education (E-Learning) for Cisco System internal engineering group. Authored several classes on the new Cisco router operation system IOS to allow engineers to develop and adapt products. Architect of Design team that designed and developed new IOS for of Cisco Routers which allows for online upgrades and new feature additions without rebooting. Developed and filed patent for new high speed routing process.

. . . . . .

March 1998 to November 1998 - **Applied Process Technology Inc., Redwood Shores, CA**
Independent Consultant

Designed and developed embedded real time control system for water treatment system. Designed power distribution, distributed I/O configuration and selected object based software for real time control. Selected and projected managed other consultant groups to design, build and ship 1000 gpm water treatment system. System control was designed for object based graphical user interface from either onsite or remote control via Internet or phone voice commands. System had automatic error detection with remote paging support. The HiPOx-1000 system is used for cleaning hazardous organic compounds from city water supplies to provide clear drinking water. The system uses high-powered ozone generators injected into a hydrogen peroxide mixture to remove volatile organic compounds. From design to first customer ship (FCS) required only 6 months.

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July 1993 to February 1998 – **TV Interactive Corporation, San Jose, CA, Founder**
Vice President Technology, Engineering and Manufacturing

Designed and developed embedded user interfaces for interactive TV. Filed over 30 patents. Developed standard for infrared communications for consumer electronics devices (IrDA). Managed engineering and manufacturing group in the development of several products for Sega, JVC, NTT, Intel and other large companies. Designed, patented and developed Windows 3.1, 95, 98, NT4 and NT5 drivers to allow CD applications to automatically start when a CD is inserted into a PC – and end the application when the CD is removed. Designed and developed serial, keyboard, and USB infrared receiver circuit, firmware and drivers for Windows 3.1, 95, 98, NT4, and NT5 for both unidirectional and bidirectional wireless keyboards, pointing devices, SmartCard, and paper-based remote controls. Designed, developed and manufactured 3D Joystick for Sega Saturn sold by Sega. Designed developed and manufactured a wireless paper-based remote control karaoke book for Japan PC sold by NTT Japan. Development of hardware including circuit design, PCB layout and 8-bit microcontroller firmware to interface with Windows PC platform. Wrote several Windows drivers to interface with Windows kernel. Developed

applications using ActiveX and DirectShow written in Visual Basic, Visual C++, and assembly. Developed Internet server (IIS) and Multimedia layout and video display tools and applications.

Management Experience: Built, managed an engineering development team (over thirty) and a manufacturing / QA team (over 15 with international manufacturing turnkey facilities) to build and deliver products to Intel, NTT, Sega, JVC. Represented and chaired committee the company in international standard organization IEC, IEEE, IRDA, DVD Standards.

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March 1993 to June 1993 – **KnowledgeWare, Inc., Redwood City, CA**
Independent Consultant

Responsible for design, implementation and conversion of a Windows-based CASE software product to Windows NT, converted software base from C to a C++ object-base system. Also added an open ended API for the support of new communications protocols.

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April 1992 to March 1993 – **Acume Technologies, Inc., Menlo Park, CA,**
Founder and Director System Engineering

Responsible for designing and prototyping of a semiconductor process module. Developed and executed project plan for building prototype system. Developed a plan for manufacturing. Completed a Bill of Materials along with full documentation. Installed company's computers, software and network. Designed User Interface using OOP's Windows-base system. Interfaced with all venders and customers.

October 1988 to April 1992 – **Novellus System Inc., San Jose, CA**
Member Technical Staff / Software Manager

Architecture and project manager for Concept II cluster tool. Chair of the SEMI/MESC control and communication task force. Project manager for new product OOP's control system. Task force member for new process development team. Implemented AI Expert-based system diagnostics. Interacted with customers to develop new features. Designed user interface for all new Novellus systems. Reported directly to Sr. VP of Technology. Responsible for Concept One Software and control system enhancements. Installed and managed an in-house LAN and MIS VAX / ASK system for accounting and manufacturing. Developed test and release procedures for software and new products. Solved customer process problems with system enhancements.

Management experience: Built and managed software (15) and electrical (8) engineering groups. Represented the company in international standard organization Semi.

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July 1984 to Sept. 1988 – **DCA / FORTE, San Jose, CA**
Staff Consultant / Manager Software Development

Designed future DCA products. Provided development support for all DCA products including coax CUT, COAX DFT, BSC, ASC, SNA, LU6.2, SRPI, SSA, Routers, SNA Gateway, X.25 and LANs. Responsible for Host to PC software and hardware product design, development and support. Managed staff to develop several Host to PC products. Developed, wrote and supported both Host and PC high-speed file transfer and virtual disk products. Implemented Incident tracking system for product support.

Director of data processing staff to install and maintained a multi-host data center with international access. Designed and developed an OS/2 Communication Manager.

Management experience: Built and managed three software development teams (26) and Mainframe MIS 9) groups. Create product plans and reported monthly status to the CEO.

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Jan. 1985 to Sept. 1985 – **Indisys, San Jose, CA, Founder**
Sr. Consulting Engineer

Designed and developed a PC-based FM single sideband mail service for ABC and Epson (Lotus signal). Developed the hardware, software and microcode (BIOS) for this real-time on-line service. System included central host computer with uplink to satellite, which injected the real-time data onto an FM station transmitter sideband carrier. Satellite downlink data was received by a PC and written to disk or printer. Designed hardware and software including low-level microcode interface.

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Feb. 1979 to June 1984 – **Amdahl Corporation, Sunnyvale, CA**
Senior Staff System Engineer

Duties were to provide consulting services to Amdahl customers and Product Support division. Headed VM tools project including conversion and testing VM and MVS modifications. Developed, wrote, and presented classes on VM, MVS and 580 hardware from usage to internals. Project managed VM and MVS performance measurement for customers. Provided technical support in debugging customer's problems for Amdahl support centers. Consulted in development and quality control of Amdahl products. Consulted and tuned for Amdahl benchmarks. Project managed Amdahl's internally developed software for field tools support. Member of 580 microcode, macrocode bringup team and design group for 580 VLSI packaging.

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August 1978 to Feb. 1979 – **American National Insurance, Galveston, Texas**
System Programmer

Duties were to install, maintain and tune an on-line VM/MVS host computer system for the insurance inquiry.

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April 1976 to August 1978 – **University of Kentucky Computer Center, Lexington, KY**
System Programmer

Duties included installation of new software system, updating and maintaining existing in-house operating system (VM, MVT, DOS). Planning, installation, and maintaining statewide teleprocessing equipment. Responsible for system and user backup of University's IBM 370 complex.

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April 1975 to March 1976 – **Ohio Institute of Technology, Columbus, Ohio**
Part-time Computer Operator

Responsible for morning start-up and general system operation of in-house IBM 1130 system. Ran students' programs, consulted with students. Responsible for running production student grading system and end-of-semester programs.

System Hardware and Software:

Host Hardware:

IBM - 3390, 3380, all 3270 related communication, 3745, 3725, 3725, 4705, 3705, 2703, 580 CPU's, 470 CPU's, 9370, 4361, 4381, 4341, 3090, 3081, 3033, 370/168, 370/165, 370/125, 360/67, 1800, 1130, 407, 402, DEC 11/780, 3600, CRAY MP, IBM and Amdahl Super Computers.

PC Hardware:

Cisco Routers, PC/104, PS/2, COMPAQ, PC/AT, PC/XT, PC, Pentium, 80486, 80386, 80286, 80186, 8088, Mac II, Mac SE, 68000, 6800, Multibus, VMX, STD.

PC Software:

Windows XP, SE, ME, CE, 95/ 98/ NT 4 -5/ CE, OS/2 PM & CM, MS/DOS, QNX, IBM/DOS, Lotus 123, Microsoft Word, WordPerfect, Designer, Gem, Project, AutoCAD, Photoshop, Protel.

Host Software:

MVS/ESA, VM/XA, MVS/XA, VMS, ASK System, VM/SP, MVVS/SP, DOS/VSE, DOS/SP, UNIX, JES2, JES3, TSO, ISPF, CMS, JCL, VM/370, MVT/HASP, MFT/ASP, CP/67.

Communications Products and Protocols:

GSM, CDMA, GPRS, UTMS, All Cisco routers and Internet protocols, IrDA FIR/SIR, CIR, UIR, Novell NetWare Networks, Several Gateway systems, Routers, Bridges, WAN, OSI, 3Com products, TCP/IP, FDDI, NETBIOS, TokenRing, Ethernet, ASN.1, GOSIP, Arcnet, BaseBand, FiberNet, BroadBand, SNA, Sniffer, ISDN, VTAM, SNA, ECF, PEP, SRPI, VCNA, NPSI, EP, NCP.

Languages:

OOP's system development, Microsoft C++, JAVA, J2ME, MSDN SDK, MSDN DDK, SmallTalk, Several Modeling Packages Host and PC based, Expert System, Microsoft C, Lattice C, Turbo C, PVCS, SMP, BDASE, Excel, Lotus, Script, GDDM, SAS, 370 / 390 BAL, 808xx Assemble, 68000 Assembly, Lisp, Basic, PL/1, PL/M, Fortran, Cobol.

Personal:

Marital Status: Single
Place of birth: Lexington, Kentucky, USA
Height: 5' 11"
Weight: 148 Lbs.
Hobbies: Scuba Diving, Chess, Karate, Water Skiing, Photography.

Organization Memberships: IEEE, AEA, SHARE, GUIDE, SEMI, MESC, IrDA, EIA, DVD.

Chairman MESC (Modular Equipment Standard Committee);
Chairman of Semi Cluster Tools Standards Group;
Chairman of IRDA Consumer Standards Group;
Wrote DVD standards (interactive index record format);
Wrote Communication Standards for Cluster Tools;
Wrote Standards for Cluster Tools computer interfaces; and
Wrote Infrared Consumer Standards Protocol.

Education:

April 1976 to June 1977 – University of Kentucky, Lexington, Kentucky
Incomplete BS degree in Electronic Engineering

Sept. 1973 to March 1976 – Ohio Institute of Technology, Columbus, Ohio,
Associated degree Electronic Engineering

May 1973 – Tates Creek High School, Lexington, Kentucky

Granted Patents

Patent Number	Date Issued	Title
US 7,047,537	May 16,2006	Code Linking System (Cisco).
US 6,968,151	Nov. 22,2005	Remote Control (Smartpaper).
US 6,650,867	Nov. 18,2003	Remote control apparatus and method of transmitting data to a host device.
US 6,642,552	Nov. 4,2003	Inductive storage capacitor (Grail).
US 6,418,532	July 9,2002	Host device equipped with means for starting a process in response to detecting insertion of a storage media.
US 6,327,459	Dec. 4, 2001	Remote control with a detachable insert.
US 6,249,863	June 19,2001	Host device equipped with means for starting a process in response to detecting insertion of a storage media.
US 5,973,313	Oct. 26, 1999	Method and apparatus for generating ratiometric control signals
US 5,957,695	Sept. 28, 1999	Structure and method for displaying commercials and sending purchase orders by computer
US 5,911,582	June 15, 1999	Interactive system including a host device for displaying Information remotely controlled by a remote control
US 5,847,694	Dec. 8, 1998	Apparatus for generating a signal indicative of the position of a movable element in the apparatus
US 5,839,905	Nov. 24, 1998	Remote control for indicating specific information to be displayed by a host device.
US 5,825,284	Oct. 20, 1998	System and method for the detection of vehicle rollover Conditions.
US 5,818,037	Oct. 6, 1998	Controller using a flexible element to vary light transferred to a photosensitive element.
US 5,795,156	August 18, 1998	Host device equipped with means for starting a process in response to detecting insertion of a storage media.
US 5,788,507	August 4, 1998	Method for remotely controlling a display of information from a storage media.
US 5,757,304	May 26, 1998	Remote control including an integrated circuit die supported by a printed publication and method for forming the remote control.
US 5,749,735	May 12, 1998	Interactive book, magazine and audio/video compact disk box.
US 5,711,672	Jan. 27, 1998	Method for automatically starting execution and ending execution of a process in a host device based on insertion and removal of a storage media into the host device.
US 5,650,608	July 22, 1997	Method and apparatus for generating ratiometric control signals.
US 5,624,265	April 29, 1997	Printed publication remote control for accessing interactive media.
US 5,597,307	Jan.28, 1997	Method for starting up a process automatically on insertion of a storage media into a host device.

2 patents issued in China
1 patent in Korea
1 Patent in Japan

Pending Patents

File Number	Date submitted	Title
xx/xxx,xxx	Nov., ,2009	Object Based File Systems
xx/xxx,xxx	Nov., ,2009	Database Verify and Update
xx/xxx,xxx	Nov., ,2009	FRAMES and their Functions
xx/xxx,xxx	Oct, ,2009	Architecture Independent Objects
xx/xxx,xxx	Oct, ,2009	Messaging Routing and Object Passing in a Distributed Network
xx/xxx,xxx	Oct, ,2009	Variable Length Data Fields
xx/xxx,xxx	Oct, ,2009	VPI Machine Architecture
xx/xxx,xxx	August, ,2009	Visual Programming Interface
xx/xxx,xxx	August, ,2009	Data addressing using bytesets
xx/xxx,xxx	August. 2009	Reverse Data Addressing
61/xxx,xxx	August,2009	Turbine Electoral Generator
61/227,581	July 22,2009	Solar Powered Plasma Hydrogen Generator
61/167,115	April 6,2009	Solar Panel with Lens and Reflector
11/739,639	April 24,2007	Message Push with pull of information to a communication computing device
60/810,769	June 2, 2006	Message push with pull of information to a communcations computer device
11/739,638	April 24, 2007	Formatting and compressuin of content data
11/739,644	April 24, 2007	Method and System for Linking to content and services for a communication device
11/758,188	May 25, 2007	Information Broadcast system and method
60/809,983	June 1, 2006	System and Method for Multicasting information to one or more computing devices
M-2725-3P	Dec. 19, 1994	Position sending method and apparatus.
M-2725-4P	July 26, 1994	Position sensing controller and method for generating control signals.
M-2725-5P	August 31, 1994	Infrared communication apparatus and method between a controller and a controlled device.
M-2726-2P	June 30, 1995	Method for automatically stopping software.
M-2726-3D	Oct. 31, 1995	An interactive book, magazine and audio/ video compact disk box.
M-2726-5D	Feb. 15, 1996	An interactive book, magazine and audio video compact disk box for purchasing on the internet.
M-2726-6D	Nov. 1, 1995	Interactive device using a host computer.
M-2726-8D	Nov. 2, 1995	Interactive development system software.
M-4046	April 9, 1996	A controller using a flexible element to vary light transfer to a photosensitive element.
M-4068	Sept. 18, 1997	CyberAd commercial insertion.
M-4142	June 20, 1996	Interactive Settop box.
M-4162	August 6, 1996	A method for using a comb structure to form a touch panel.
M-4338	March 13, 1997	A interactive activity switch for displaying content.
M-4483	Sept. 13, 1996	Flip chip Die supported by paper printed with conductive ink.
M-4527	Dec. 19, 1996	UPC printed overlay.
M-5086	August 20, 1997	A toy based remote control and method of using the remote control.
CISCO	Dec. 15, 1999	Fast path switching using imbedded jump tables.
Grail Semi	Dec. 2003	Inductive storage capacitor – allowed
Grail Semi	Dec. 2003	Inductive storage capacitor - allowed
AskMeNow	Feb 2006	Provisional prepared for real time SMS info lookup.

GMT	June 2006	Click through process for mobile ADs and email reply.
GMT	June 2006	Data formatting into mobile format GML (GPC) files.
GMT	June 2006	Real time push of internet data to the screen of the mobile device.
GMT	June 2006	Broadcast to multiple mobile phones at the one time (mobile multicast).
GMT	May 2007	Security on a mobile device using off system key used to encrypt data that will be send to a mobile device and is unlocked and displayed by the mobile device.
GMT	May 2007	Icon based identifier to allow mobile device user to verify and certify data content publisher.
GMT	Dec 2007	IP broadcast using SMS only system.
GMT	Feb 2008	Mobile content conversion and reformatting of data content based on a mobile device profile used to resize and shape displayable content.
GMT	March 2008	Cursor appears when moving and disappears when not moving.
GMT	March 2008	Video wall paper
GMT	March 2008	GML email format (this allows for non blackberry like email on any mobile device.
GMT	March 2008	Ads profiling and being added as content is format and pushed
GMT	April 2008	A short range base station for mobile wallet transaction.
GMT	April 2008	Java on the sim to allow for the reinstall of the application if the user moves the sim to a new phone.
GMT	April 2008	Push trigger and phone to phone session binding using IP tunneling.
GMT	April 2008	Mobile device to device application interface and programs (calendar, phone book, chat, many others)

EXHIBIT D

US005596529A

United States Patent [19]

Noda et al.

[11] Patent Number: 5,596,529

[45] Date of Patent: Jan. 21, 1997

[54] **NONVALATILE SEMICONDUCTOR MEMORY DEVICE**

[75] Inventors: **Junichiro Noda**, Tokyo; **Daisuke Tohyama**, Kawasaki, both of Japan

[73] Assignee: **Kabushiki Kaisha Toshiba**, Kawasaki, Japan

[21] Appl. No.: **351,185**

[22] Filed: **Nov. 30, 1994**

[30] **Foreign Application Priority Data**

Nov. 30, 1993 [JP] Japan 5-299951

[51] **Int. Cl.**[6] **G11C 11/34**

[52] **U.S. Cl.** **365/185.28**; 257/314; 257/316; 257/317; 257/318; 257/370

[58] **Field of Search** 365/185.28; 257/314, 257/316, 377, 318, 320

[56] **References Cited**

U.S. PATENT DOCUMENTS

4,794,562	12/1988	Kato et al.	365/182
5,066,992	11/1991	Wu et al.	357/23.5
5,282,161	1/1994	Villa	365/185.28

FOREIGN PATENT DOCUMENTS

0256993	2/1988	European Pat. Off. .
0443515	8/1991	European Pat. Off. .
63-84168	4/1988	Japan .

OTHER PUBLICATIONS

The 13th Annual IEEE Nonvolatile Semiconductor Workshop, J. Noda et al., "A Novel EEPROM Cell for High Density Application and Single Power Supply Power Operation", Feb. 20–22, 1984.

IEDM Tech. Dig., pp. 26–29, 1988, R. Shirota et al., "An Accurate Model of Subbreakdown Due to Band–to–Band Tunneling and Its Application".

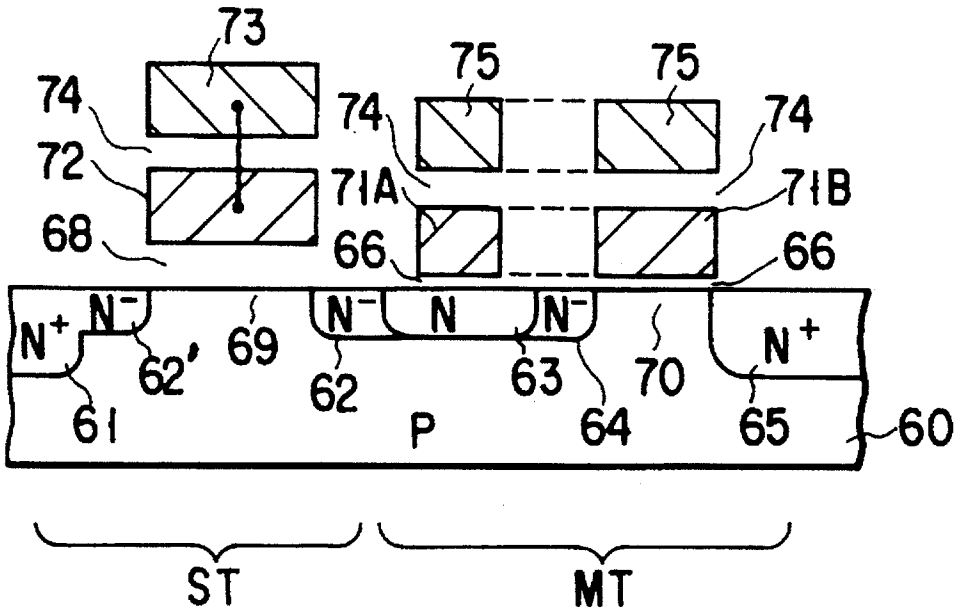
IEDM Tech. Dig., pp. 24–27, 1981, J. R. Yeargain et al., "A High Density Floating–Gate EEPROM Cell".

Primary Examiner—David C. Nelms
Assistant Examiner—F. Niransam
Attorney, Agent, or Firm—Banner & Witcoff, Ltd.

[57] **ABSTRACT**

A select MOS transistor and a data storage MOS transistor are formed in an element region. The transistor has floating-gate electrodes. The floating-gate electrodes are spaced apart above the element region and connected to each other above a field region. Only a tunnel insulating film much thinner than a gate insulating film of the transistor is placed between the floating-gate electrode and a drain region. Only the gate insulating film much thinner than the gate insulating film of the transistor is placed between the floating-gate electrode and the channel region of the transistor. In the element region, the shape of a control electrode is the same as that of the floating-gate electrodes.

23 Claims, 11 Drawing Sheets



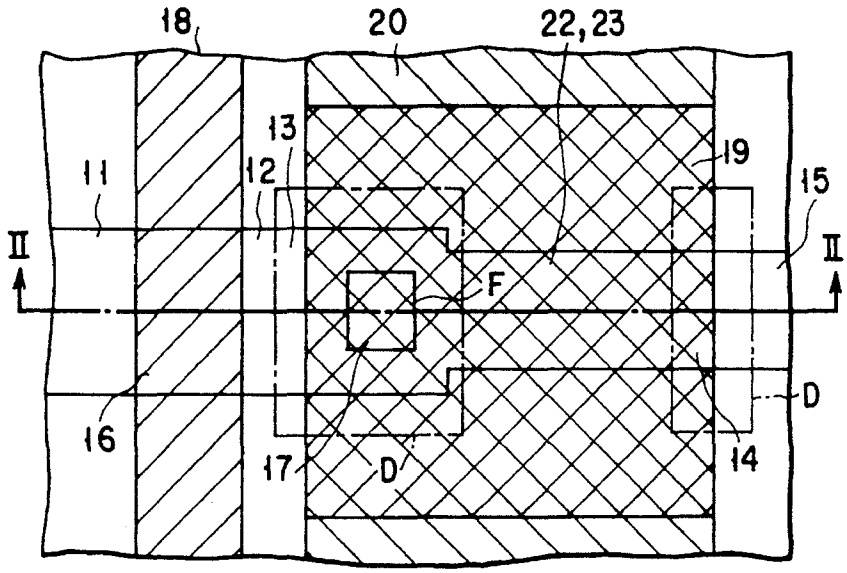


FIG. 1
(PRIOR ART)

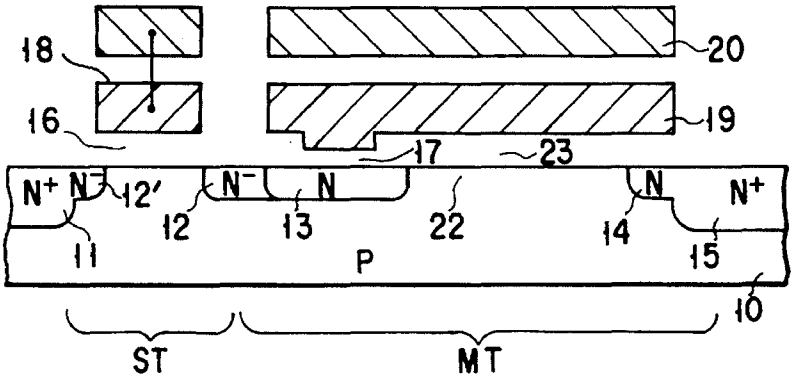


FIG. 2
(PRIOR ART)

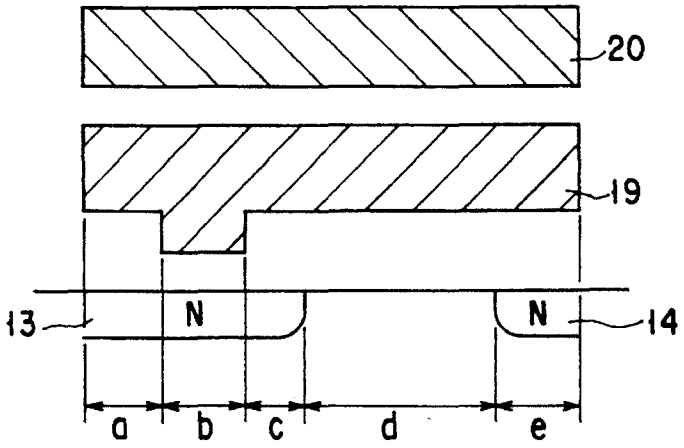


FIG. 3
(PRIOR ART)

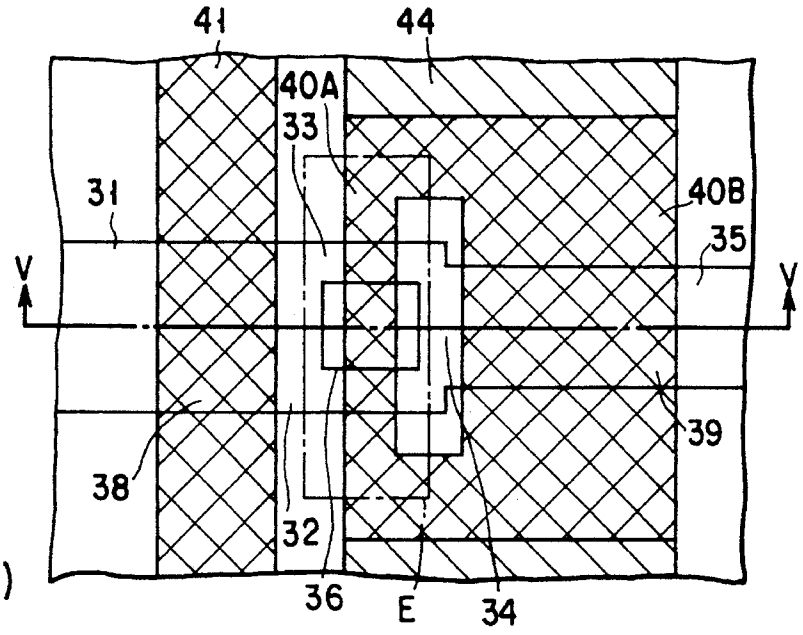


FIG. 4
(PRIOR ART)

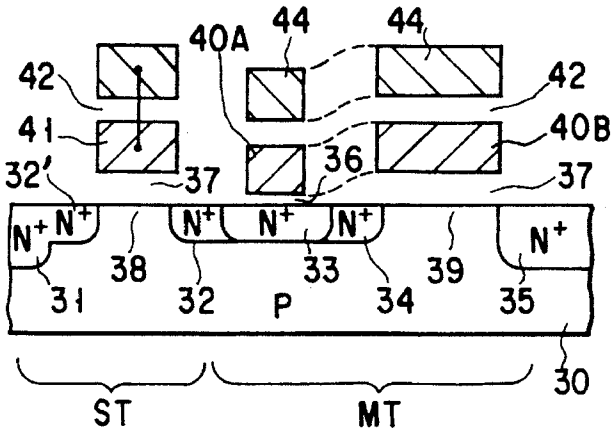


FIG. 5
(PRIOR ART)

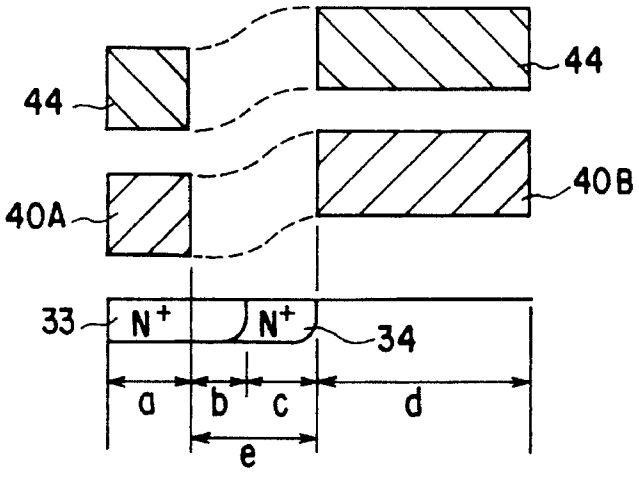


FIG. 6
(PRIOR ART)

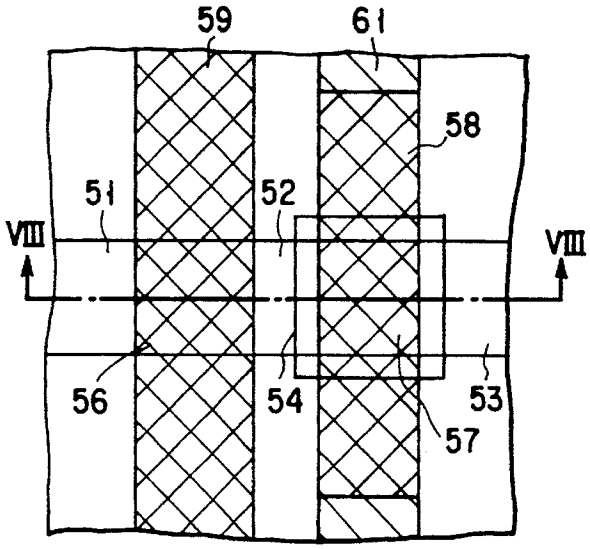


FIG. 7 (PRIOR ART)

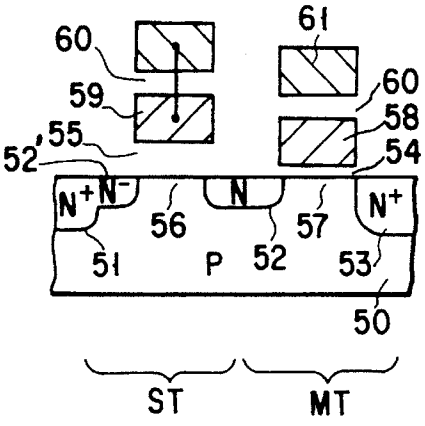


FIG. 8 (PRIOR ART)

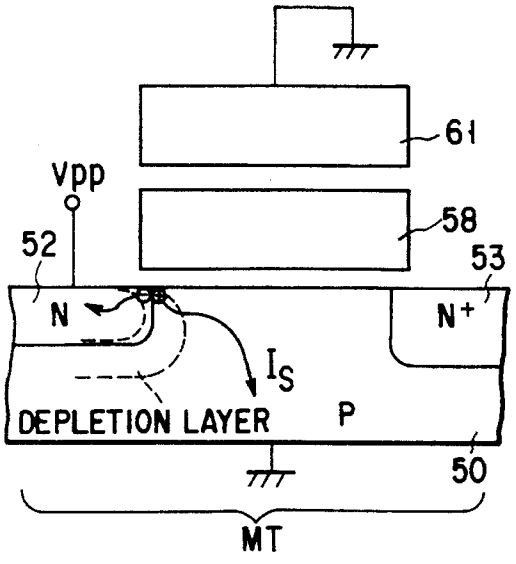


FIG. 9 (PRIOR ART)

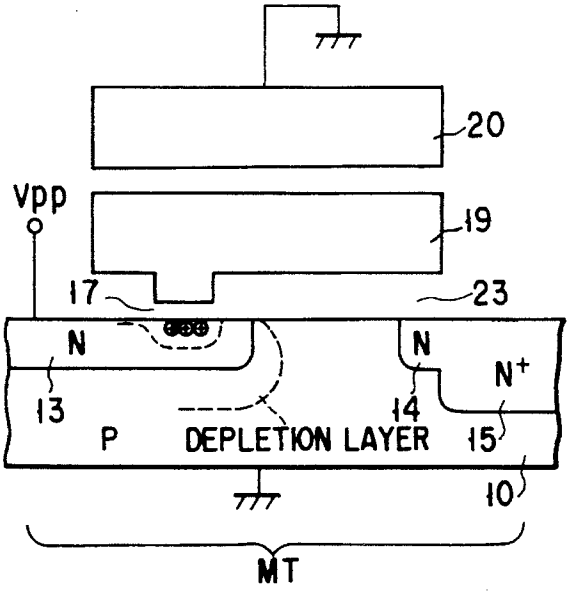


FIG. 10 (PRIOR ART)

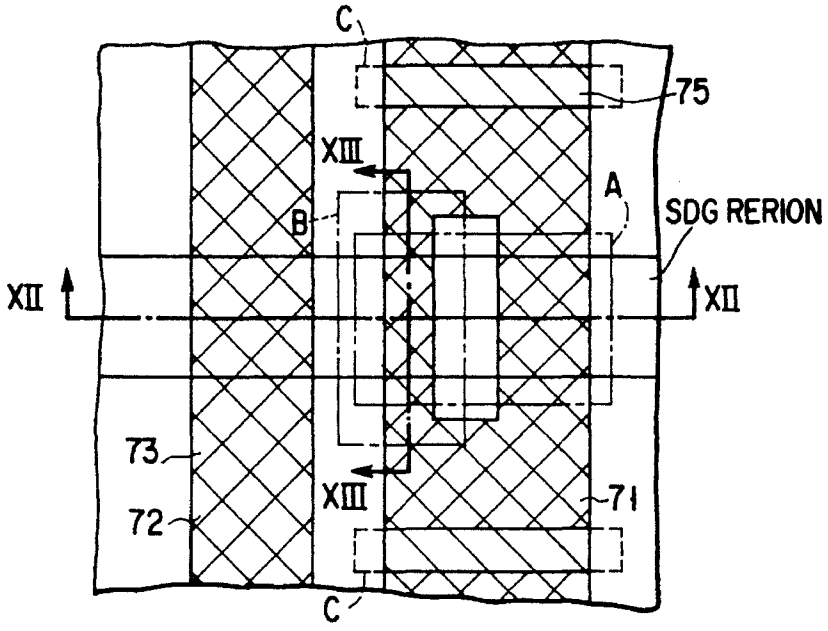


FIG. 11

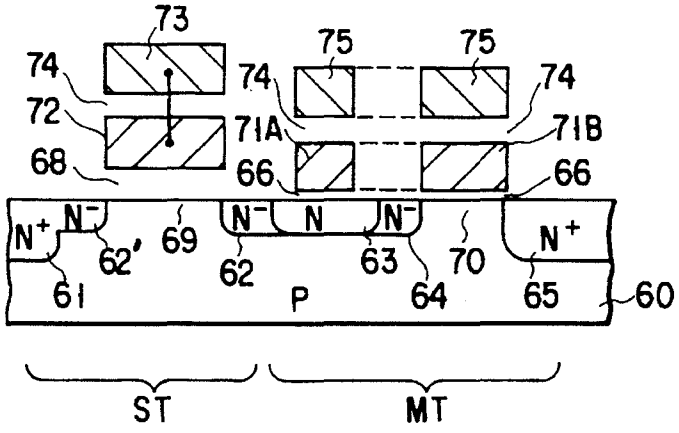


FIG. 12

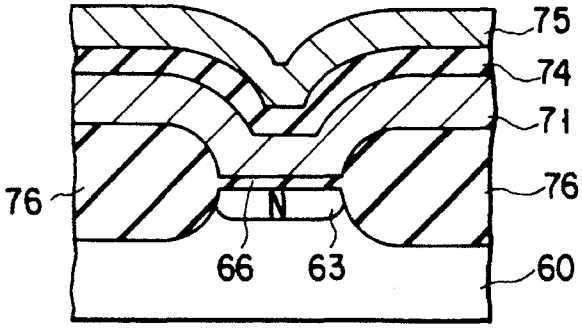


FIG. 13

FIG. 14

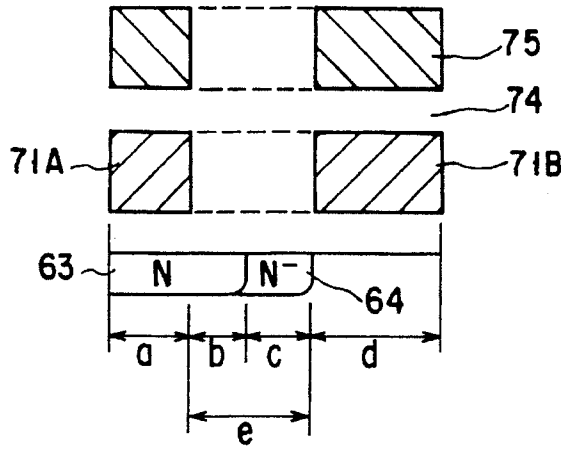


FIG. 15

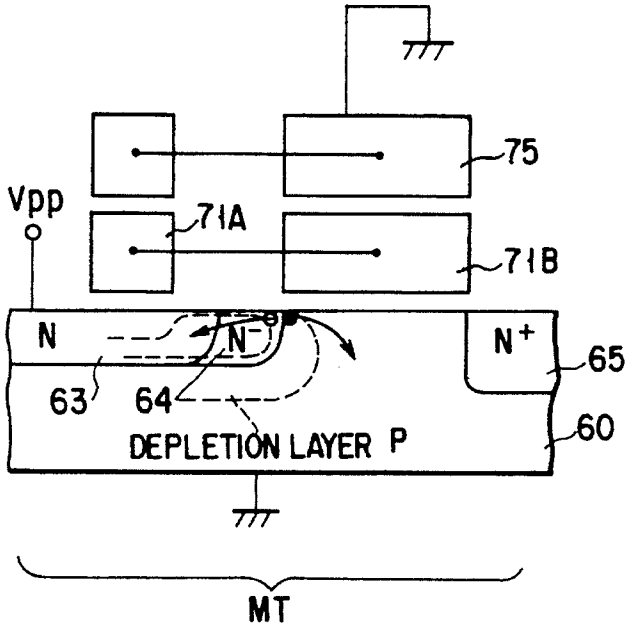
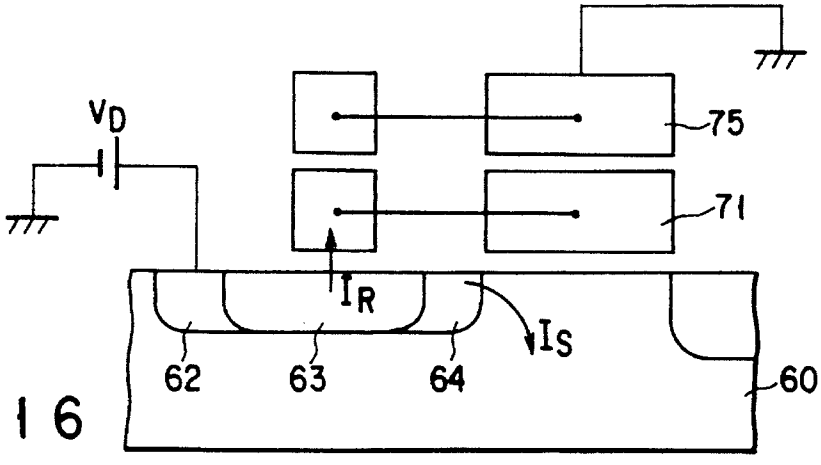


FIG. 16



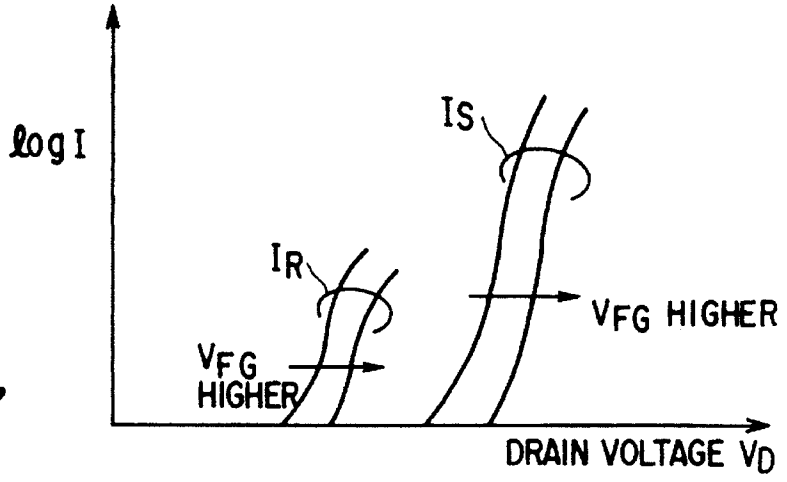


FIG. 17

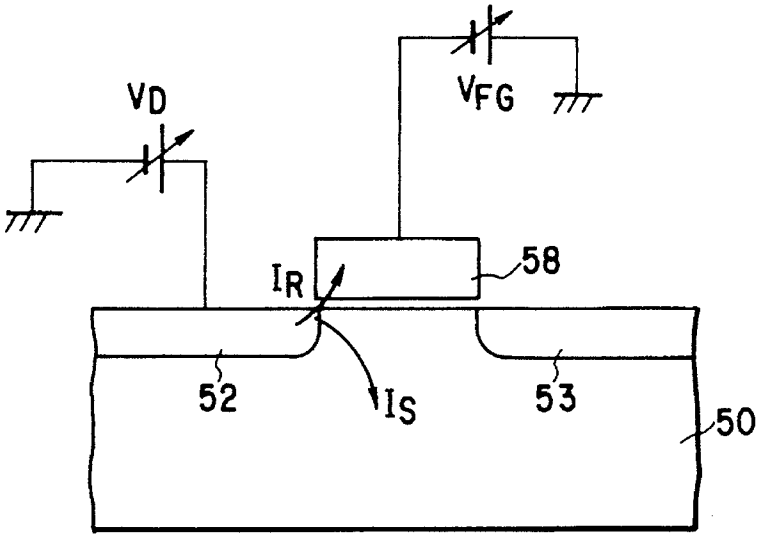


FIG. 18

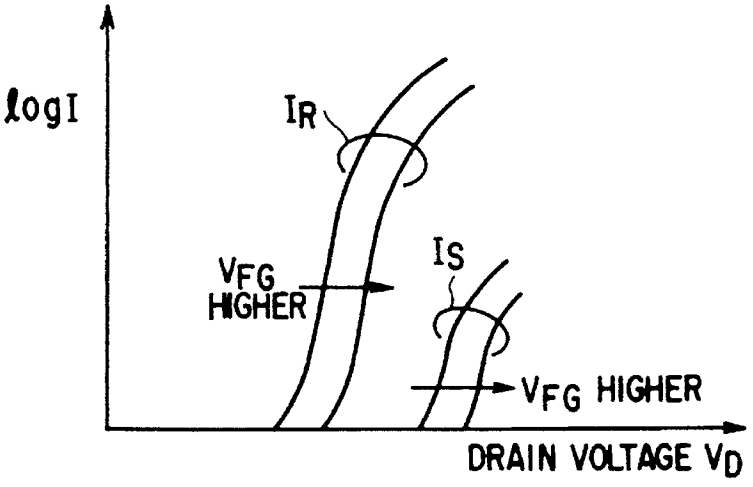


FIG. 19

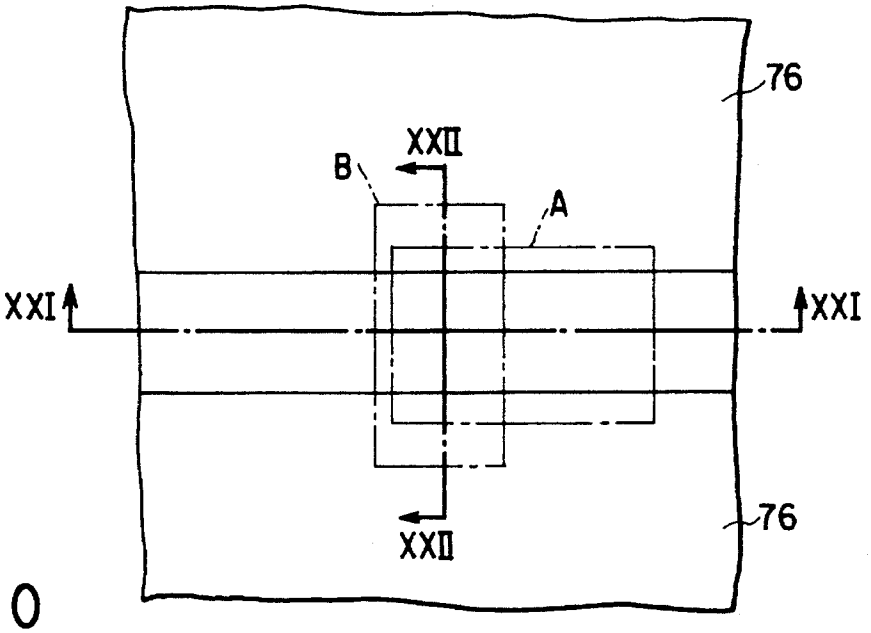


FIG. 20

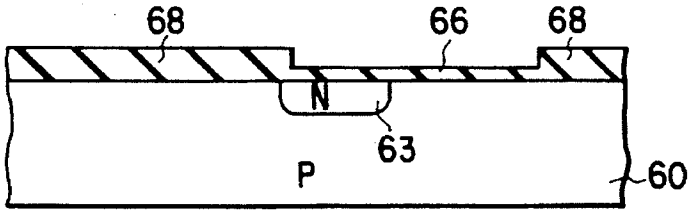


FIG. 21

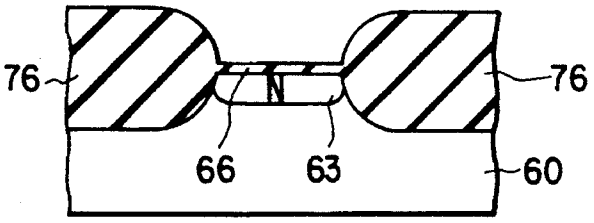


FIG. 22

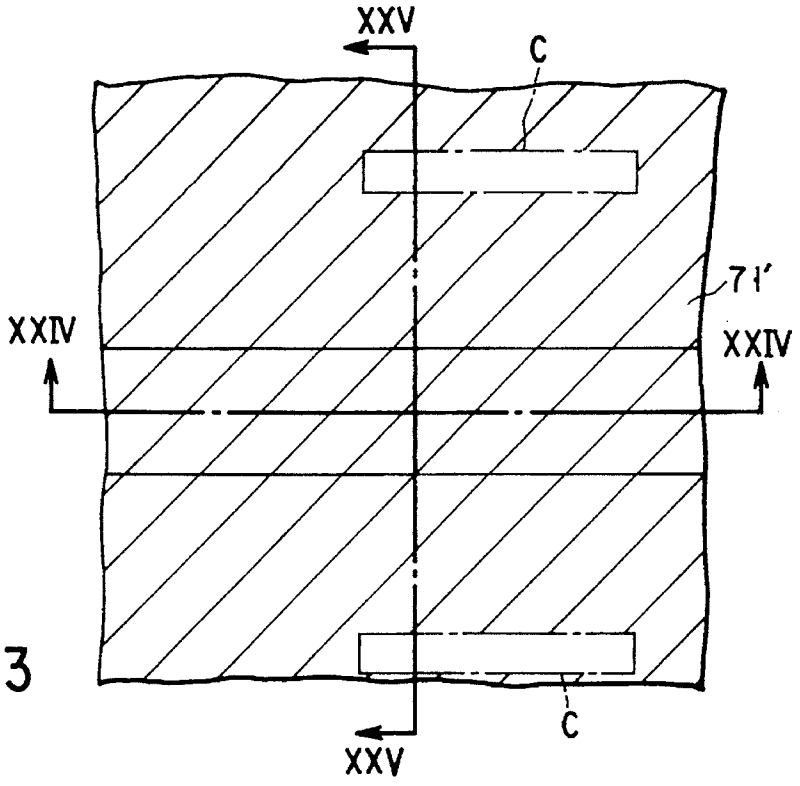


FIG. 23

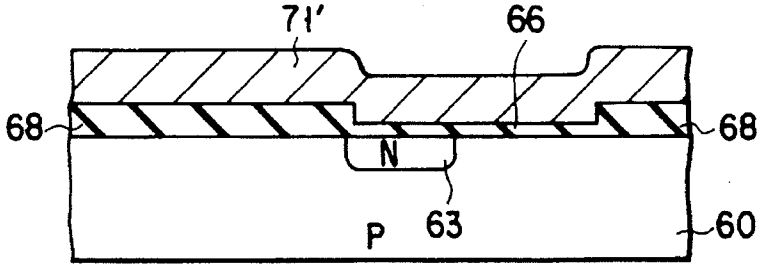


FIG. 24

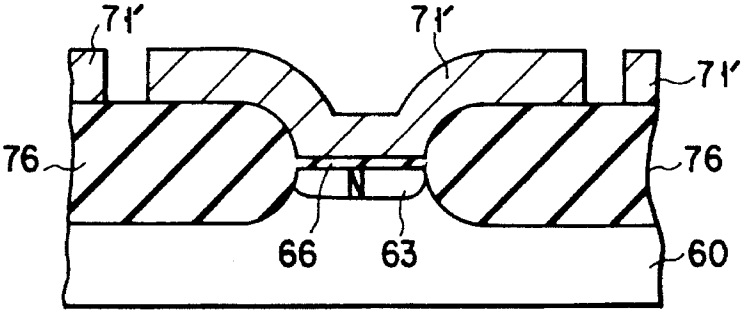


FIG. 25

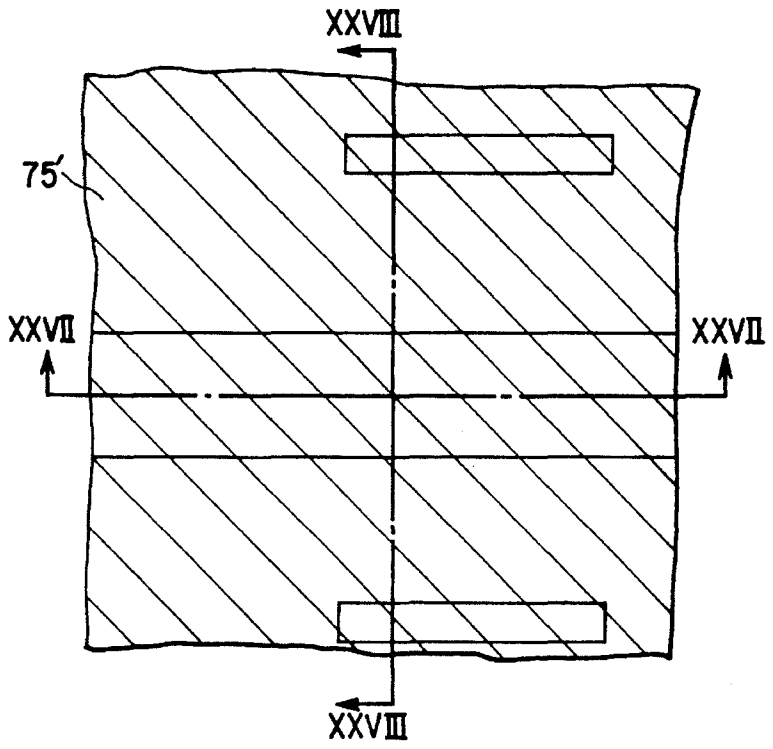


FIG. 26

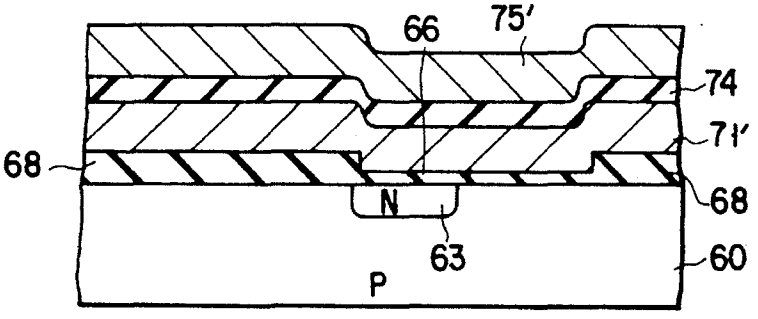


FIG. 27

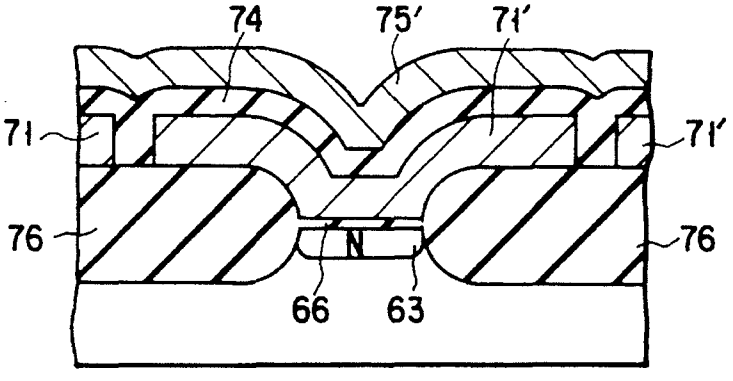


FIG. 28

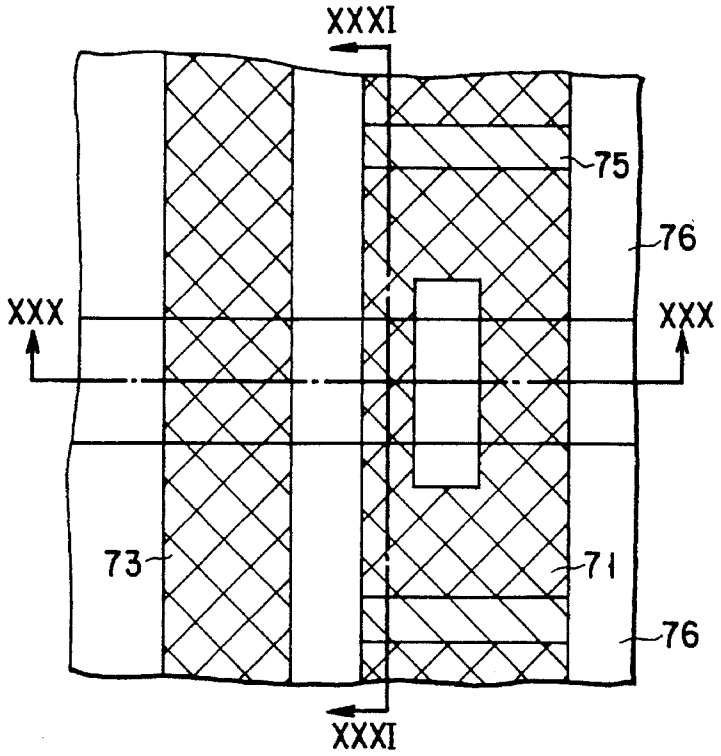


FIG. 29

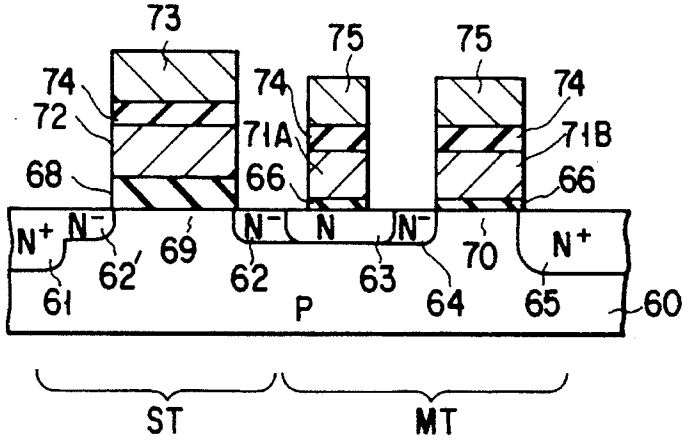


FIG. 30

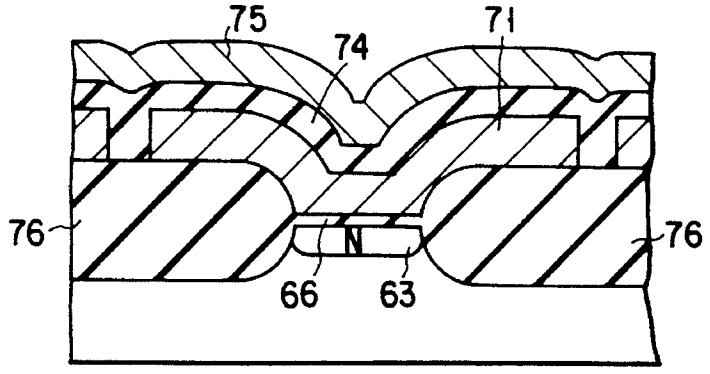


FIG. 31

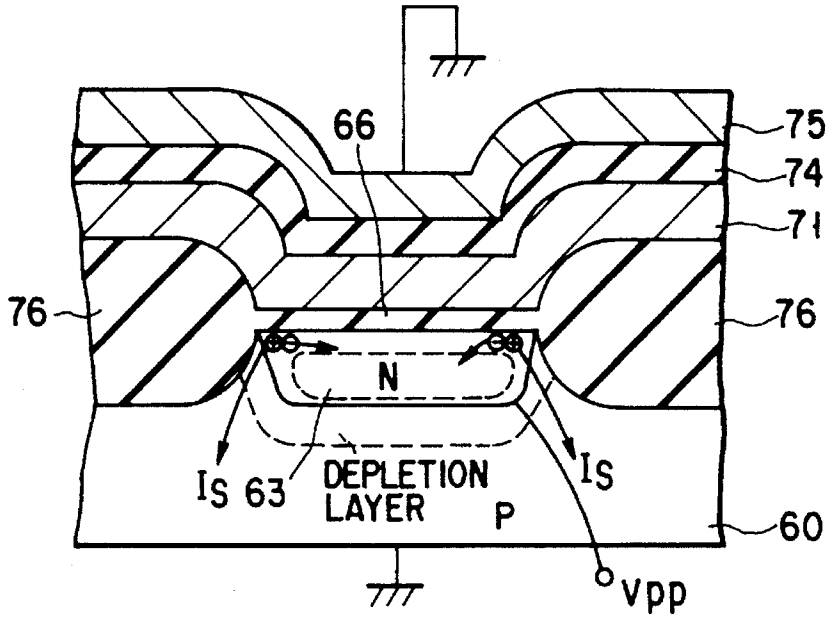

66
75
74
71
76
76
N
IS 63
DEPLETION LAYER
P
IS
60
Vpp

FIG. 32

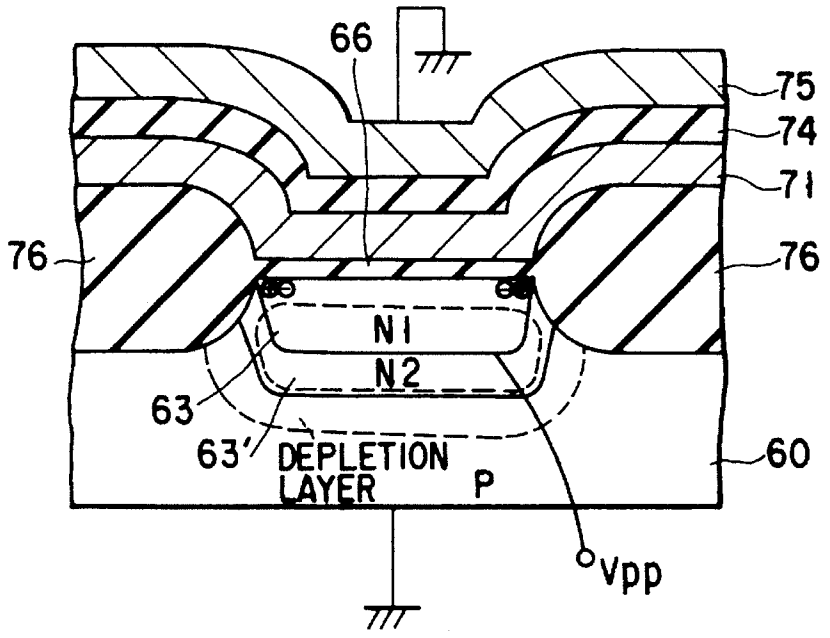

66
75
74
71
76
76
N1
N2
63
63'
DEPLETION LAYER
P
60
Vpp

FIG. 33

NONVALATILE SEMICONDUCTOR MEMORY DEVICE

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates to a nonvolatile semiconductor memory device capable of electrically rewriting data and semipermanently retaining data.

2. Description of the Related Art

Nonvolatile semiconductor memory devices using double-gate MOS transistors with a floating gate and a control gate are well known.

A conventional nonvolatile semiconductor memory device will be explained with reference to FIGS. **1** to **10**.

FIGS. **1** and **2** show a first structure of a conventional nonvolatile semiconductor memory device.

The nonvolatile semiconductor memory device is of the most widely used type. FIG. **1** is a plan view of a memory cell in the nonvolatile semiconductor memory device. FIG. **2** is a sectional view taken along line II–II' of FIG. **1**.

The memory cell is composed of a data storage MOS transistor MT and a select MOS transistor ST, which are connected to each other in series.

The source region of the select MOS transistor ST and the drain region of the data storage MOS transistor MT are made up of n-type regions **12** and **13** at the surface of a p-type semiconductor substrate **10**, respectively.

On a partial surface of the n-type region, a very thin silicon oxide film **17** of nearly 10 nm in thickness is formed. A floating-gate electrode **19** and a control gate electrode **20** are formed on and above the channel region **22** of the data storage MOS transistor MT and the silicon oxide film **17**. The floating-gate electrode **19** and control gate electrode **20** are made of polysilicon, for example.

In a place directly under the floating-gate electrode **19** where the silicon oxide film **17** has not been formed, and directly under the gate electrode **18** of the select MOS transistor ST, silicon oxide films **23**, **16** (of several tens nm) several times as thick as the silicon oxide film **17** are formed.

The drain region of the select MOS transistor ST is composed of n-type regions **11**, **12'**, and the source region of the data storage MOS transistor MT is made up of n-type regions **14**, **15**.

With the memory cell of such a configuration, the erasing of data is effected by applying a high potential to the control gate electrode **20** of the data storage MOS transistor MT. Specifically, once a high potential has been applied to the control gate electrode **20**, Fowler-Nordheim tunneling allows electrons to move from the n-type region (drain region) **13** via the silicon oxide film **17** to the floating-gate electrode **19**.

The writing of data is performed by applying a high potential to the n-type region (drain region) **11** and the gate electrode **18** of the select MOS transistor ST, and 0 V to the control gate electrode **20** of the data storage MOS transistor MT. As a result, the n-type regions (drain region) **12**, **13** of the data storage MOS transistor MT are at a high potential, so that the tunnel effect allows electrons to move from the floating-gate electrode **19** to the drain region via the silicon oxide film **17**.

Hereinafter, the source region and drain region of the memory cell will be described.

The n-type region (drain region) **13** of the data storage MOS transistor is formed directly under the floating-gate electrode **19** before the floating-gate electrode **19** is formed. On the other hand, the n-type region (source region) **15** of the data storage MOS transistor MT is formed in a self-aligning manner by implanting n-type impurities into the substrate **10** using the floating-gate electrode **19** and control gate electrode **20** as a mask.

when only the n-type region **15** is the source region, however, the channel length of the data storage MOS transistor MT is the distance between the n-type region **13** and the n-type region **15**. Therefore, the channel length of the data storage MOS transistor MT varies depending on the misalignment of the mask for forming the n-type region **13** from the mask for forming a polysilicon mask used in forming the n-type region **15**.

Since the change of the channel length of the data storage MOS transistor MT results in a change in the characteristics of the memory cell, it is not desirable to form only the source region in a self-aligning manner.

To avoid this problem, the following method is generally used: before the floating-gate electrode **19** is formed, n-type impurities are implanted into region D enclosed by a dot-dash line in FIG. **1**, thereby forming the n-type region **13** and n-type region **14** at the same time.

with this method, the channel length of the data storage MOS transistor MT is the distance between the n-type region **13** and the n-type region **14**. Since the n-type regions **13**, **14** are formed with the same mask, the channel length of the data storage MOS transistor MT is always constant. As a result, the channel length of the data storage MOS transistor MT will not vary due to mask misalignment.

However, this method has a disadvantage in that, to assure the formation of the n-type region **14** directly under the floating-gate electrode **19**, the floating-gate electrode **19** must be lengthened along the channel length of the data storage MOS transistor MT, by the sum of the amount of misalignment of the mask for forming the floating-gate electrode **19** and the amount of misalignment of the mask for forming the n-type regions **13**, **14**.

Hereinafter, the thin silicon oxide film **17** of nearly 10 nm in thickness between the n-type region **13** and the floating-gate electrode **19** will be examined.

The silicon oxide film **17** is formed by removing the thick silicon oxide films **16**, **23** of several tens nm in thickness using a mask with an opening in area F in FIG. **1** and then performing thermal oxidation.

The thin silicon oxide film **17** must be formed on the n-type region **13** and directly under the floating-gate electrode **19**. This causes a disadvantage: the floating-gate electrode **19** must be lengthened along the channel length by the sum of the amount of misalignment of the mask for forming the floating-gate electrode **19** from the mask for forming an opening in area F and the amount of misalignment of the mask for forming an opening in area F from the mask for forming the n-type region **13**.

To sum up, the minimum dimension along the channel of the data storage MOS transistor MT in the memory cell is determined as shown in FIG. **3**.

Specifically, the minimum dimension along the channel of the data storage MOS transistor MT is determined by the sum of the following:

The amount of alignment of the mask for forming the floating-gate electrode **19** and control electrode **20** from the mask for forming an opening in area F where the silicon oxide film **17** is to be formed (expressed by "a")

The length of area F where the silicon oxide film **17** is to be formed (expressed by "b")

The amount of misalignment of the mask for forming an opening in area F where the silicon oxide film **17** is to be formed from the mask for forming the n-type region **13** (expressed by "c")

The channel length of the data storage MOS transistor MT (expressed by "d")

The amount of misalignment of the mask for forming the n-type region **14** from the mask for forming the floating-gate electrode **19** and the control gate **20** (expressed by "e")

The memory cell of the structure shown in FIGS. **1** and **2** requires a lot of misalignments to be taken into account in designing, as compared with an ordinary MOS transistor having a self-aligning structure, and therefore has the disadvantage of resulting in larger memory cells.

Explained next will be the thickness of the gate oxide film of the data storage MOS transistor MT.

To withstand high voltages in a write operation or an erase operation, the gate oxide film of the select MOS transistor ST is several times as thick as the gate oxide film of a MOS transistor to which only an ordinary power-supply voltage (e.g., 5 V) is applied.

The gate oxide film of the data storage MOS transistor MT and the gate oxide film of the select MOS transistor ST are formed simultaneously. As a result, the gate oxide film of the data storage MOS transistor MT is as thick as the gate oxide film of the select MOS transistor ST.

To make the data storage MOS transistor MT smaller, it is necessary to make its gate oxide film as thin as possible. As mentioned above, the gate oxide film of the data storage MOS transistor MT is as thick as the gate oxide film of the select MOS transistor ST, that is, several times as thick as the gate oxide film of an ordinary MOS transistor. For this reason, the channel length of the data storage MOS transistor MT is larger than the channel length of an ordinary MOS transistor.

As described above, in the case of the memory cell shown in FIGS. **1** and **2**, because a lot of misalignments have to be taken into account and a larger channel length is required, the cell area will become larger.

The potential of the floating gate when a high potential is applied to the drain region is determined by the capacitive coupling between the drain region and the floating gate. In the case of the memory cell of the above structure, the capacitive coupling between the drain region and the floating gate of the data storage MOS transistor MT varies according to the misalignment of the mask for forming the n-type region **13** from the mask for forming the floating-gate electrode **19**. The variation in the capacitive coupling results in a variation in the amount of electrons released from the floating-gate electrode into-the drain region.

Accordingly, this causes variations in the threshold voltage of the data storage MOS transistor MT after electrons have been released.

FIGS. **4** and **5** show a double structure of a conventional nonvolatile semiconductor memory device. FIG. **4** is a plan view of a conventional nonvolatile semiconductor memory device. FIG. **5** is a sectional view taken along line V–V'.

The conventional nonvolatile semiconductor memory device has been disclosed in Jpn. Pat. Appln. KOKAI Publication No. 63-84168.

With this conventional device, it is possible to solve the problem with the conventional device shown in FIGS. **1** and **2**, that is, it is possible to suppress variations in the write characteristics of the memory cell due to mask misalignment.

As with the conventional device of FIGS. **1** and **2**, the memory cell is composed of a data storage MOS transistor MT and a select MOS transistor ST, which are connected to each other in series.

Above the channel region **39** of the data storage MOS transistor MT, a first portion **40**B of a floating-gate electrode is provided via a gate insulating film **37** of several tens nm in thickness.

On a partial surface of the drain region **33** of the data storage MOS transistor MT, a gate insulating film **36** of nearly 10 nm in thickness (much thinner than the gate insulating film **37**) is provided. On the gate insulating film **36**, a second portion **40**A of the floating-gate electrode is provided.

Although the first portion **40**B and second portion **40**A of the floating-gate electrode are spaced apart, they are electrically connected to each other above a field region. On and above the first portion **40**B and second portion **40**A of the floating-gate electrode, an insulating film **42** and a control gate electrode **44** are provided. It is preferable that the shape of the control gate electrode **44** should be the same as that of the floating-gate electrode.

The source region of the select MOS transistor ST and the drain region of the data storage MOS transistor are made up of n-type regions **32**, **33**, **34** formed continuously at the surface of a p-type semiconductor substrate **30**. The drain region of the select MOS transistor ST is made up of n-type regions **31**, **32'**, and an n-type region **35** is the source region of the data storage MOS transistor MT.

In such a memory cell, too, the n-type region **33** is formed before the formation of the floating-gate electrode and control gate electrode, as with the conventional device of FIGS. **1** and **2**.

In this case, the n-type region **33** is formed by implanting n-type impurities into area E of the substrate **30** enclosed by a dot-dash line in FIG. **4**. On the other hand, the n-type regions **32'**, **32**, **34** are formed in a self-aligning manner by implanting n-type impurities into the substrate **30** using the floating-gate electrodes **40**A, **40**B and control gate electrode **44** as a mask. The n-type regions **31**, **35** are formed by implanting n-type impurities into the substrate **30** using a specific mask.

With this conventional device, there arises a misalignment of the mask for forming the floating-gate electrodes **40**A, **40**B and a misalignment of the mask for forming the n-type region **33**.

In the case of this conventional device, however, even if such mask misalignments take place, this will cause no variations in the capacitive coupling between the n-type regions (drain region) **32** to **34** of the data storage MOS transistor MT and the floating-gate electrodes **40**A, **40**B.

The reason for this is that the capacitive coupling between the n-type regions (drain region) **32** to **34** and the floating-gate electrodes **40**A, **40**B is determined by the area of the portion where the n-type region (drain region) **33** overlaps with the second portion **40**A of the floating-gate electrode and the area is constant regardless of mask misalignment.

Consequently, with the memory cell in the conventional device, the write characteristics of the memory cell will not vary due to mask misalignment.

Furthermore, with the conventional device, the n-type regions **34**, **35** can be formed in a self-aligning manner using the floating-gate electrodes **40**A, **40**B and control gate electrode **44** as a mask. Therefore, it is not necessary to take into account a misalignment of the mask for forming the n-type regions **34**, **35** and a misalignment of the masks for forming the floating-gate electrodes **40**A, **40**B and control gate electrode **44**.

To sum up, in the memory cell in the conventional memory cell, the minimum dimension along the channel length of the data storage MOS transistor MT is shown in FIG. **6**.

Specifically, the minimum dimension along the channel length of the data storage MOS transistor MT is determined by the sum of the following:

The length of the second portion **40**A of the floating-gate electrode (expressed by "a")

The amount of misalignment of the mask for forming the n-type region **33** from the mask for forming the floating-gate electrodes **40**A, **40**B (expressed by "b" and "c")

The channel length of the data storage MOS transistor MT (expressed by "d")

However, when the minimum spacing (expressed by "e") in which the floating-gate electrode and control gate electrode (polysilicon) can be processed is greater than b+c, the minimum dimension is determined by a+d+e.

Hereinafter, the conventional device in FIGS. **1** and **2** is compared with the conventional device in FIGS. **4** and **5**.

If a, b, c, and d in FIG. **3** are almost equal to c, a, b, and d in FIG. **6**, the data storage MOS transistor MT of FIG. **6** can be made smaller by the length of e. As a result, with the conventional device of FIGS. **4** and **5**, the dimensions of a memory cell can be made smaller than those of a memory cell in the conventional device of FIGS. **1** and **2**.

However, in the memory cell in the conventional device of FIGS. **4** and **5**, the thickness of the gate oxide film **37** of the data storage MOS transistor MT is larger. Accordingly, the channel length of the data storage MOS transistor MT is larger, so that the area of the memory cell cannot be made much smaller than that of the memory cell in the conventional device of FIGS. **1** and **2**.

To overcome this shortcoming, a third structure of a conventional nonvolatile semiconductor memory device has been proposed in John R. Yeargain & Clinton Kuo, "A High Density Floating-Gate EEPROM Cell," IEDM Technical Digest, December, 1981.

FIG. **7** shows a third structure of a conventional nonvolatile semiconductor memory device. FIG. **8** is a sectional view taken along line VIII–VIII' of FIG. **7**.

The memory cell is composed of a data storage MOS transistor MT and a select MOS transistor ST, which are connected to each other in series.

The source region of the select MOS transistor ST and the drain region of the data storage MOS transistor MT are composed of an n-type region **52** formed at the surface of a p-type semiconductor substrate **50**. On the entire surface of the channel region **57** of the data storage MOS transistor MT, a thin silicon oxide film **54** of nearly 10 nm in thickness is formed. On the thin silicon oxide film **54**, a floating-gate electrode **58** made of polysilicon is formed. On and above the floating-gate electrode **58**, an insulating film **60** and a control gate electrode **61** are formed.

Directly under a gate electrode **59** of the select MOS transistor ST, an insulating film much thicker than the silicon oxide film **54**, for example, a silicon oxide film **55** of nearly several tens nm in thickness, is formed.

The drain region of the select MOS transistor ST is composed of n-type regions **51**, **52'**, and an n-type region **53** is the source region of the data storage MOS transistor MT.

With the memory cell of such a structure, the erasing of data is performed by applying a high potential to the control gate electrode **61** of the data storage MOS transistor MT. Once a high potential has been applied to the control gate electrode **61** of the data storage MOS transistor MT, Fowler-Nordheim tunneling allows electrons to move from the n-type region (drain region) **52**, channel region **57**, and n-type region (source region) **53** via the silicon oxide film **54** to the floating-gate electrode **58**.

The writing of data is performed by applying a high potential to the n-type region (drain region) **51** and gate electrode **59** of the select MOS transistor ST, and 0 V to the control gate electrode **61** of the data storage MOS transistor MT. As a result, the n-type region (drain region) **52** of the data storage MOS transistor MT are at a high potential, so that the tunnel effect allows electrons to move from the floating-gate electrode **58** to the n-type region (drain region) **52** via the silicon oxide film **54**.

with the structure of the memory cell, the n-type regions **52'**, **52**, **53** are formed in a self-aligning manner using the gate electrode **59** of the select MOS transistor ST, the floating-gate electrode **58** and control gate **61** of the data storage MOS transistor MT as masks, respectively.

The thin silicon oxide film **54** is formed on the entire surface of the channel region of the data storage MOS transistor MT.

Therefore, unlike the conventional device of FIGS. **1** and **2** and that of FIGS. **4** and **5**, it is not necessary to take into account the misalignment of the mask for forming the n-type regions **52'**, **52**, **53** from the mask for forming the floating-gate electrode and the misalignment of the mask for specifying an area in which a silicon oxide film is to be formed from the mask for forming the floating-gate electrode.

Since the gate oxide film of the data storage MOS transistor MT is as thin as nearly 10 nm, the channel length can be made very small.

For the reasons described above, the area of the memory cell is much smaller than that in the conventional device of FIGS. **1** and **2** and that in the conventional device of FIGS. **4** and **5**.

It is known that in a MOS device with a thin oxide film, a breakdown phenomenon takes place due to band-to-band tunneling. The phenomenon has been described in detail in R. Shirota, T. Endoh, M. Momodomi, R. Nakayama, S. Inoue, R. Kirisawa & F. Masuoka, "An Accurate Model of Subbreakdown due to Band-to-Band Tunneling and its Application," IEDM, 1988.

The phenomenon will be explained briefly.

For instance, with an n-channel MOS transistor, when a voltage higher than the gate voltage is applied to its source or drain, a depletion layer at the surface of the source or drain overlapping with the gate electrode expands. The phenomenon of electrons tunneling from the valence band to the conduction band, or what is called a band-to-band tunneling phenomenon, has occurred, and at the surface, electrons and holes are generated. Then, as the electrons move to the drain and the holes move to the substrate, thus, a substrate current develops.

In a conventional device in FIGS. **7** and **8**, a thin oxide film **54** is formed on the entire surface of the channel region of a data storage MOS transistor MT.

As shown in FIG. **9**, when a high potential is applied to the n-type region (drain region) of the data storage MOS transistor MT in a write operation, a depletion layer at the surface of the n-type region (drain region) **52** overlapping with a floating-gate electrode **58** expands, allowing a substrate current Is to flow through band-to-band tunneling.

On the other hand, with the conventional device of FIGS. **1** and **2**, as shown in FIG. **10**, the gate oxide film **23** of the data storage MOS transistor MT is as thick as several tens nm, and one end of the n-type region (drain region) of the data storage MOS transistor MT is under the thick gate oxide film **23**.

This prevents the depletion layer at the surface at the end of the n-type region (drain region) **13** from expanding further. Because the depletion layer at the surface acts as a potential barrier, the holes generated at the surface at the end of the n-type region **13** do not move to the substrate, and a substrate current due to band-to-band tunneling does not flow.

In the conventional device of FIGS. **4** and **5**, a substrate current will not develop because of similar reasons.

In a nonvolatile semiconductor memory device which electrically write and erase data, high potentials necessary for a write operation and an erase operation are generated at the step-up circuit in the LSI, in some cases.

With the device of FIGS. **7** and **8**, since a large substrate current develops during a write operation, it is difficult to cause the step-up circuit in the LSI to supply a high potential (a write current). Especially, at the time of a page rewrite operation in which data should be written into many memory cells. The writing of data may not be carried out.

A substrate current during a write operation increases the power consumption in the LSI. Therefore, in the case of an LSI required to be less power-consuming, such as a battery-powered LSI, the generation of substrate current is not desirable. That is, the conventional device of FIGS. **7** and **8** has the following disadvantage: although the cell area can be made very small, a substrate current flows due to band-to-band tunneling in a write operation, thus preventing a high potential from being generated within the LSI, with the result that a less power-consuming operation cannot be achieved.

As described above, the conventional nonvolatile semiconductor memory devices have disadvantages in that when they are designed to make smaller the drawn current during a write operation, the area of the memory cell becomes larger, and in that, conversely, when they are designed to make the area of the memory cell much smaller, the drawn current during a write operation becomes larger.

SUMMARY OF THE INVENTION

Accordingly, the object of the present invention is to provide a nonvolatile semiconductor memory device the area of whose memory cell is small and in which the drawn current during a write operation is small, thereby enabling high integration of memory cells, a step-up operation in the LSI, and a less power-consuming operation.

The foregoing object is accomplished by providing a nonvolatile semiconductor memory device comprising: a semiconductor substrate with an element region and a field region; a select MOS transistor formed in the element region; and a data storage MOS transistor formed in the element region.

The data storage MOS transistor contains a source region, a drain region, a floating-gate electrode, and a control gate electrode. The floating-gate electrode is composed of a first portion above the drain region and a second portion above the semiconductor substrate between the source region and the drain region. Between the drain region and the first portion and between the semiconductor substrate and the second portion, only an insulating film thinner than a gate insulating film of the select MOS transistor is placed. The first portion and the second portion are spaced apart above the element region and connected to each other on the field region.

The drain region of the data storage MOS transistor contains: a first region which is placed in a region including a place directly under the first portion, and one end of which is on the bottom of a spacing between the first portion and the second portion; and a second region one end of which is placed on the side of the second portion, and the other end of which is connected to one end of the first region, and whose impurity concentration is set more than several times lower than the impurity concentration in the first region.

The first region is composed of impurities of more than two types whose diffusion coefficient differs from each other. The impurities whose diffusion coefficient is lower than the remaining ones of the impurities of more than two types determine the impurity concentration at the surface of the drain region of the data storage MOS transistor, and the impurities whose diffusion coefficient is higher than the remaining ones of the impurities of more than two types extend to directly under the field region.

A method of manufacturing nonvolatile semiconductor memory devices according to the present invention, comprises the following steps:

First, a first region is formed by implanting impurities of a second conductivity type into an element region of a semiconductor substrate of a first conductivity type, and a first insulating film is formed in the element region.

Then, the first insulating film on the first region and a region adjacent to the first region is removed, and a second insulating film thicker than the first insulating film is formed on the semiconductor substrate exposed in the element region.

Then, a first conducting film is formed on the entire surface of the semiconductor substrate, a slit-like hole is formed in a specified position of the first conducting film, a third insulating film is formed on the entire surface of the semiconductor substrate, and a second conducting film is formed on the third insulating film.

Thereafter, the second conducting film, the third insulating film, the first conducting film, the second insulating film, and the first insulating film are etched in sequence, so as to form a gate electrode of the select MOS transistor and a control gate electrode and a floating-gate electrode of the data storage MOS transistor. The control gate electrode and the floating-gate electrode have a first portion and a second portion above the element region. The first portion is placed above the first region. The first portion and the second portion are spaced apart on the element region and connected to each other on a field region.

Next, impurities of a second conductivity type are implanted into the element region with the gate electrode of the select MOS transistor and the control gate electrode and floating-gate electrode of the data storage MOS transistor as a mask, so as to form a second region in the element region between the first portion and the second portion and a third region in the element region between the first portion and the gate electrode of the select MOS transistor.

With the above-described configuration, an insulating film much thinner than the gate insulating film of the select MOS transistor directly under the first portion and second portion of the floating-gate electrode.

Because of this, the channel length of the data storage MOS transistor can be shortened. Since the first and second portions of the floating-gate electrode are spaced apart, an impurity region for determining the channel length of the data storage MOS transistor can be formed in a self-aligning manner. Therefore, the memory cell can be made smaller.

Furthermore, the drain region of the data storage MOS transistor contains the first region formed directly under the first portion of the floating-gate electrode and the second

region formed between the first region and the second portion of the floating-gate electrode. The impurity concentration in the second region is more than several times lower than that in the first region.

As a result, a substrate current can be prevented at one end of the drain region along the channel length of the data storage MOS transistor during a write operation. Namely, only a write current is allowed to flow, resulting in a smaller drawn current.

Additionally, the first region is composed of impurities of more than two types whose diffusion coefficient differs from each other. The impurities whose diffusion coefficient is lower determines the impurity concentration at the surface of the drain region, and the impurities whose diffusion coefficient is higher extends to directly under the field region.

Consequently, a substrate current can be prevented at one end of the drain region across the channel width of the data storage MOS transistor during a write operation. Namely, only a write current is allowed to flow, resulting in a smaller drawn current.

As described above, not only can a smaller memory cell area and a lower drawn current in a write operation be achieved, but a step-up operation within the LSI and a lower power-consuming operation can also be performed.

Additional objects and advantages of the invention will be set forth in the description which follows, and in part will be obvious from the description, or may be learned by practice of the invention. The objects and advantages of the invention may be realized and obtained by means of the instrumentalities and combinations particularly pointed out in the appended claims.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings, which are incorporated in and constitute a part of the specification, illustrate presently preferred embodiments of the invention, and together with the general description given above and the detailed description of the preferred embodiments given below, serve to explain the principles of the invention.

FIG. **1** is a plan view of a conventional nonvolatile semiconductor memory device;

FIG. **2** is a sectional view taken along line II–II' of FIG. **1**;

FIG. **3** is a sectional view of the data storage MOS transistor in the device of FIG. **2**;

FIG. **4** is a plan view of a conventional nonvolatile semiconductor memory device;

FIG. **5** is a sectional view taken along line V–V' of FIG. **4**; FIG. **6** is a sectional view of the data storage MOS transistor in the device of FIG. **4**;

FIG. **7** is a plan view of a conventional nonvolatile semiconductor memory device;

FIG. **8** is a sectional view taken along line VII–VII' of FIG. **7**;

FIG. **9** is a view of an expanse of a depletion layer in the drain region during a write operation in the device of FIG. **7**;

FIG. **10** is a view of an expanse of a depletion layer in the drain region during a write operation in the device of FIG. **1**;

FIG. **11** is a plan view of a nonvolatile semiconductor memory device according to the present invention;

FIG. **12** is a sectional view taken along line XII–XII' of FIG. **11**;

FIG. **13** is a sectional view taken along line XIII–XIII' of FIG. **11**;

FIG. **14** is a sectional view of the data storage MOS transistor in the device of FIG. **11**;

FIG. **15** is a view of an expanse of a depletion layer in the drain region during a write operation in the device of FIG. **11**;

FIG. **16** shows the relationship between drain voltage V_D, write current I_R, and substrate current Is in FIG. **11**;

FIG. **17** shows the relationship between drain voltage V_D, write current I_R, and substrate current Is in FIG. **11**;

FIG. **18** shows the relationship between drain voltage V_D, write current I_R, and substrate current Is in FIG. **7**;

FIG. **19** shows the relationship between drain voltage V_D, write current I_R, and substrate current Is in FIG. **7**;

FIG. **20** is a plan view of a process in a method of manufacturing nonvolatile semiconductor memory devices according to the present invention;

FIG. **21** is a sectional view taken along line XXI–XXI' of FIG. **20**;

FIG. **22** is a sectional view taken along line XXII–XXII' of FIG. **20**;

FIG. **23** is a plan view of a process in a method of manufacturing nonvolatile semiconductor memory devices according to the present invention;

FIG. **24** is a sectional view taken along line XXIV–XXIV' of FIG. **23**;

FIG. **25** is a sectional view taken along line XXV–XXV' of FIG. **23**;

FIG. **26** is a plan view of a process in a method of manufacturing nonvolatile semiconductor memory devices according to the present invention;

FIG. **27** is a sectional view taken along line XXVII–XXVII' of FIG. **26**;

FIG. **28** is a sectional view taken along line XXVIII–XXVIII' of FIG. **26**;

FIG. **29** is a plan view of a process in a method of manufacturing nonvolatile semiconductor memory devices according to the present invention;

FIG. **30** is a sectional view taken along line XXX–XXX' of FIG. **29**;

FIG. **31** is a sectional view taken along line XXXI–XXXI' of FIG. **29**;

FIG. **32** is a view of an expanse of a depletion layer in the drain region during a write operation in the device of FIG. **11**; and

FIG. **33** is a view of an expanse of a depletion layer in the drain region during a write operation in the device of FIG. **11**.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Hereinafter, referring to the accompanying drawings, a nonvolatile semiconductor memory device according to the present invention will be explained in detail.

FIGS. **11** to **13** show the main portion of a nonvolatile semiconductor memory device of the present invention. FIG. **11** is a plan view of the structure of a memory cell used in the nonvolatile semiconductor memory device of the invention. FIG. **12** is a sectional view taken along line

XII–XII'. FIG. **13** is a sectional view taken along line XIII–XIII'.

The memory cell is composed of a select MOS transistor ST and a data storage MOS transistor MT with a floating-gate electrode and a control gate electrode, these two transistor being connected to each other in series.

Numeral **60** is a p-type silicon semiconductor substrate, for example. The surface region of the substrate **60** is made up of an SDG region (source, drain, and gate regions) and a field region. In the SDG region of the substrate **60**, n-type regions **61**, **62'**, **62**, **63**, **64**, **65** and channel regions **69**, **70** are formed.

On the field region of the substrate **60**, a very thick silicon oxide film **76** is formed. The n-type regions **61**, **62'** constitute the drain region of the select MOS transistor ST. The n-type regions **62**, **63**, **64** constitute the source region of the select MOS transistor ST and the drain region of the storage MOS transistor MT. These n-type regions **62**, **63**, **64** are arranged continuously in a line. The n-type region **65** is the source region of the data storage MOS transistor MT.

First, the impurity concentration in the n-type regions **62**, **63**, **64** will be explained.

The impurity concentration in the n-type region **64** is set lower than that in the n-type region **63**. For instance, the difference in impurity concentration between the n-type regions **63** and **64** is set at more than several times. Therefore, when the dosage of the n-type region **63** is approximately 5×10^{13} cm^{-2}, the dosage of the n-type region **64** is set at approximately 1×10^{13} cm^{-2}.

The impurity concentration in the n-type region **62** is not limited to a specific value or a specific range. That is, even if the impurity concentration in the n-type region **62** takes any value, the memory cell operates properly. Since making the impurity concentration in the n-type region **62** equal to that in the n-type region **64** enables the n-type region **62** and the n-type region **64** to be formed simultaneously, this helps reduce the number of manufacturing processes.

Explanation of the thin silicon oxide film **66** will be given.

On a part of the substrate where area A indicated by a dot-dash line overlaps with the SDG region as shown in FIG. **11**, a very thin silicon oxide film **66** of nearly 10 nm in thickness is formed. The silicon oxide film **66** is formed on the most surface or the entire surface of the n-type region **63**, on the n-type region **64**, and on the substrate **60** between the n-type region **64** and the n-type region **65** (on the channel region **70** of the data storage MOS transistor MT).

The silicon oxide film **66** serves not only as a path through which electrons pass during a write operation or an erase operation, but also as a gate insulating film of the data storage MOS transistor MT.

On the remaining area of the SDG region where the silicon oxide film **66** has not been formed, a silicon oxide film **68** of several tens nm in thickness is formed. The silicon oxide film **68** functions as a gate oxide film of the select MOS transistor ST.

On the n-type region **63** and on the channel region **70** of the data storage MOS transistor MT, the silicon oxide film **66** and the floating-gate electrode **71** are formed. The floating-gate electrode **71** is formed into a shape with a slit-like opening in its center.

Specifically, in the SDG region, the floating-gate electrode **71** is made up of a first portion **71A** and a second portion **71B**. The first portion **71A** and the second portion **71B** are electrically connected to each other on the field region.

To sum up, the thin silicon oxide film **66** is formed at least on a part of the. substrate **60** where the SDG region overlaps with the first and second portions **71A**, **71B** of the floating-gate electrode. Only the silicon oxide film **66** directly under the first portion **71A** of the floating-gate electrode acts as a tunnel insulating film, whereas only the silicon oxide film **66** directly under the second portion **71B** of the floating-gate electrode acts as a gate insulating film.

On and above the channel region **69** of the select MOS transistor ST, the silicon oxide film **68** of nearly several tens nm in thickness and a gate electrode **72** made of polysilicon are formed.

On and above the floating-gate electrode **71**, an insulating film **74** of several tens nm in thickness and a control gate electrode **75** made of polysilicon are formed. The insulating film **74** consists of a silicon oxide film, a silicon nitride film, or a laminate film of these films (e.g., an ONO film), for example. It is preferable that the shape of the control gate electrode **75** should be almost equal to the shape of the floating-gate electrode **71** in the direction in which the drain and source are arranged.

On and above the gate electrode **72** of the select MOS transistor ST, an insulating film **74** and a gate electrode **73** made of polysilicon are formed. The gate electrode **72** and the gate electrode **73** are electrically connected to each other. The gate electrode **72** virtually functions as the gate electrode of the select MOS transistor ST.

The reason why the select MOS transistor ST has a double-layered gate electrode is to form the floating-gate electrode and control electrode of the data storage MOS transistor MT and the gate electrode of the select MOS transistor ST in the same process at the same time. The two-layered gate electrode of the select MOS transistor ST has the effect of simplifying the manufacturing processes. It should be noted that even if the gate electrode of the select MOS transistor ST is designed to have a single-layer structure, the memory cell will operate properly.

Explained next will be the dimension along the channel length of the data storage MOS transistor MT in the memory cell thus constructed.

As shown in FIG. **14**, the dimension along the channel length of the data storage MOS transistor MT is determined by the sum of the following:

- The length of the first portion of the floating-gate (expressed by "a")
- The amount of misalignment of the mask for forming the n-type region **63** from the mask for forming the floating-gate (expressed by "b" and "c")
- The channel length of the data storage MOS transistor MT (expressed by "d")

When the minimum spacing "e" where the floating-gate electrode and control gate electrode (polysilicon) can be processed is larger than the sum of b and c, the dimension is determined by the sum of a, d, and e.

For the memory cell of the invention, the n-type region **64** and n-type region **65** that determine the channel length of the data storage MOS transistor MT are formed in a self-aligning manner using the floating-gate electrode **71** and control gate electrode **75** as a mask. Therefore, with the invention, the problem with the conventional device of FIGS. **1** and **2** can be avoided. Specifically, it is not necessary to take into account the misalignment of the mask for forming the n-type region (source region) **65** of the data storage MOS transistor MT from the mask for forming the floating-gate electrode **71**. Therefore, the memory cell can be made smaller by the amount of mask misalignment.

Explained next will be the channel length "d" of the data storage MOS transistor MT.

The thickness of the gate oxide film of the data storage MOS transistor MT in the conventional devices in FIGS. **1** and **2** and FIGS. **4** and **5** is nearly several tens nm, whereas the thickness of the gate oxide film of the data storage MOS transistor MT in the memory cell in FIGS. **11** to **13** is nearly 10 nm.

Therefore, according to the reduction rules of the MOS transistor, the channel length can be theoretically made several times shorter than that in the conventional device of FIGS. **1** and **2** or of FIGS. **4** and **5**. Namely, since the channel length which accounts for the largest percentage of the factors determining the dimension along the channel length of the data storage MOS transistor MT, can be reduced, the area of the memory cell can be made much smaller.

Explained next will be the dimension across the channel width of the data storage MOS transistor MT.

In the conventional device of FIGS. **1** and **2** and in that of FIGS. **4** and **5**, a very thin silicon oxide film is formed on a partial surface of the drain region of the data storage MOS transistor MT. Consequently, the width of the SDG region is inevitably made larger by the amount of misalignment of the mask for making an opening to form a silicon oxide film from the mask for forming the SDG region.

With the present invention, however, on the entire surface of the drain region of the data storage MOS transistor MT and on the entire part of the channel, a very thin silicon oxide film is formed. Therefore, the width of the SDG region can be made smaller by the amount of mask misalignment.

The spacing between adjacent SDG regions is determined by the withstand voltage between them. Therefore, reducing the dimension of the memory cell across the channel width decreases the spacing between adjacent SDG regions, thereby contributing to high integration of memory cells.

Examined next will be a substrate current in a write operation.

With the present invention, as shown in FIG. **15**, there is a slit-like opening on the edge of the n-type region **63** of high impurity concentration. That is, neither the floating-gate electrodes **71**A, **71**B nor the control gate electrode **75** exist above the edge.

Consequently, since the depletion layer does not spread much at the edge of the n-type region **63** at the surface of the substrate, a substrate current due to band-to-band tunneling as described in the conventional device of FIGS. **7** and **8** will not flow at the surface of the substrate.

On the other hand, since above the edge of the n-type region **64**, the floating-gate electrode **71**B exists, a substrate current develops. The impurity concentration in the n-type region **64** is much lower than that in the n-type region **63** (several times lower than the latter). Accordingly, the curve of the band at the edge of the n-type region **64** at the surface of the substrate is gentle, with the result that a substrate current due to band-to-band tunneling is very small.

By making the impurity concentration in the n-type region **63** as high as possible, the depletion layer at the surface of the n-type region **63** can be prevented from expanding. This makes larger the effective electric field between the drain region and the floating-gate electrode, resulting in an increase in the write current due to the tunnel effect. As a result, the writing or erasing of data can be effected easily.

Even if the impurity concentration in the n-type region **63** is made higher, a substrate current due to band-to-band tunneling does not increase as described above.

On the other hand, by making the impurity concentration in the n-type region **64** as low as possible, a tunnel current between bands decreases, thereby contributing to the reduction of power consumption. Since the write current depends on the impurity concentration in the n-type region **63**, the write current will not decrease even if the impurity concentration in the n-type region **64** is made lower.

As described above, since the write current depends only on the impurity concentration in the n-type region **63**, and the substrate current depends only on the impurity concentration in the n-type region **64**, the impurity concentration in the n-type region **63** and that in the n-type region **64** can be set at the respective optimum values. Furthermore, by setting the impurity concentration in the n-type regions **63** and **64** at the optimum values, the drain voltage at which a write current starts to flow can be set lower than the drain voltage at which a substrate current starts to flow.

Explained next will be the relationship between drain voltage V_D, write current I_R, and substrate current I_S in the data storage MOS transistor MT.

According to the present invention, by setting the impurity concentration in the n-type regions **63** and **64** at the optimum values, almost no substrate current is allowed to flow during a write operation.

As shown in FIGS. **16** and **17**, as the drain region V_D is raised, the write current I_R first flows from the drain region **63** to the floating-gate electrode **71** by the FN tunnel effect.

At this time, in the drain region V_D, almost no current Is flows because of the difference in impurity concentration between the n-type regions **63** and **64**. As the write current I_R flows, the potential of the floating-gate electrode **71** rises gradually, with the result that the potential difference between the floating-gate electrode **71** and the drain region **63** decreases gradually.

The smaller the potential difference between the floating-gate electrode **71** and the drain region **63**, the more the write current I_R due to band-to-band tunneling reduces. Therefore, the rise of the potential V_{FG} at the floating-gate electrode **71** leads to the rise of the drain voltage V_D necessary for the write current I_R to flow. At the same time, however, the drain voltage V_D at which a substrate current Is begins to flow rises as well, preventing the substrate current Is from flowing.

As described above, raising the drain voltage V_D allows sufficient write current Is to flow. The rise of the voltage VFG at the floating-gate electrode **71** results in the rise of the drain voltage V_D at which the substrate current Is starts to flow. In the end, data can be written and erased just by flowing almost no substrate current Is.

In contrast, with the conventional device of FIGS. **7** and **8**, as the drain voltage V_D is raised as shown in FIGS. **18** and **19**, the substrate current Is first starts to flow. Therefore, to write data by flowing a write current I_R, the drain voltage V_D must be raised further, resulting in higher power consumption.

Additionally, the write current I_R and substrate current Is depend only on the impurity concentration in the drain region (n-type region) **52**. As a result, the increase of the impurity concentration in the drain region **52** increases both the write current I_R and the substrate current Is, whereas the decrease of the impurity concentration in the drain region **52** decreases both the write current I_R and the substrate current Is.

Therefore, even if the n-type impurity concentration in the drain region **52** is changed in any way, the ratio of the write current I_R to the substrate current Is hardly changes with respect to the drain voltage V_D.

Normally, with the conventional device of FIGS. **7** and **8**, the drain voltage V_D at which the write current I_R starts to

flow is higher than the drain voltage V_D at which the substrate current Is starts to flow. Therefore, as the drain voltage V_D is raised, the substrate current Is first starts to flow.

Furthermore, when the drain voltage V_D is generated by an internal step-up circuit provided in the LSI, the substrate voltage reaches the voltage at which the substrate current Is balances with the current supplied from the internal step-up circuit, the rise of the drain voltage V_D stops.

Consequently, when the maximum value of the drain voltage is lower than a voltage high enough for the write current I_R to start to flow, this prevents the floating-gate potential V_{FG} from rising, making it impossible to write data. When a high voltage is supplied from an external power supply, a very large substrate current Is flows during a write operation, making it difficult to perform a low power-consuming operation.

Furthermore, when a large substrate current Is develops during a write operation, this causes disadvantages such as hot carriers being injected into the oxide film, degrading the reliability of the memory cells. Namely, a memory cell that generates a large substrate current Is as in the conventional device of FIGS. **7** and **8**, cannot improve the reliability.

However, with the present invention, by setting the impurity concentration in the n-type regions optimally, the substrate current Is during a write operation can be reduced to almost zero. Furthermore, not only an internal step-up operation but also a low power-consuming operation can be performed, thereby realizing a highly reliable memory cell.

In the embodiment, in the field regions on the right and left sides of the SDG region, the floating-gate electrodes **71**A and **71**B are connected to each other. However, in the field region only on one side of the SDG region, the floating-gate electrodes **71**A and **71**B may be connected to each other. In this case, the floating-gate electrode is formed into a U shape.

Hereinafter, a method of manufacturing nonvolatile semiconductor memory devices according to the present invention will be described.

As shown in FIGS. **20** to **22**, a field oxide film **76** is formed on a p-type silicon substrate **60**, and a SDG region and a field region are set. A silicon oxide film (not shown) formed on the SDG region. Using a mask with an opening in area B enclosed by a dot-dash line, n-type impurities are implanted into the substrate **60** to form a n-type region **63** in the region where area B overlaps with the SDG region. The silicon oxide film is removed.

A silicon oxide film **68** of nearly several tens nm in thickness is formed on the entire surface of the SDG region of the substrate **60**. Thereafter, using a mask with an opening in area A enclosed by a dot-dash line, the silicon oxide film **68** in the region where area A overlaps with the SDG region, is removed. On the region of the substrate where the silicon oxide film **68** has been removed, another thin silicon oxide film **66** of approximately 10 nm in thickness is formed.

Next, as shown in FIGS. **23** to **25**, on the entire surface of the substrate **60**, a first polysilicon layer **71'** is deposited. Then, using a mask with a slit-like opening in area C enclosed by a dot-dash line, the first polysilicon layer is selectively removed.

Next, as shown in FIGS. **26** to **28**, on the entire surface of the substrate **60**, an insulating film **74** of nearly several tens nm in thickness is formed. Then, on the insulating film **74**, a second polysilicon layer **75'** is deposited.

Then, as shown in FIGS. **29** to **31**, using a specific mask, the second polysilicon layer **75'**, the insulating film **74**, and the first polysilicon layer **71'** are etched consecutively to form floating-gate electrodes **71**A, **71**B, a control gate electrode **75**, and two layers of gate electrodes **72**, **73** for each memory cell in a selfaligning manner.

Thereafter, using the control gate electrode **75** and the gate electrode **73** as a mask, n-type impurities are implanted into the substrate **60** to form n-type regions **62**, **62'**, **64** in a self-aligning manner. At this time, the n-type regions **62**, **64** are connected to the n-type region previously formed.

Additionally, using a specific mask, n-type impurities are implanted into the substrate **60** to form n-type regions **61**, **65**.

In this way, a memory cell in a nonvolatile semiconductor memory device is completed.

With this method, the n-type regions **62**, **62'**, **64** are formed simultaneously in a self-aligning manner. This not only reduces the number of manufacturing processes, but also eliminates the necessity of taking mask misalignment into account. Furthermore, in the method, the impurity concentration in the n-type regions **62**, **62'** is equal to that in the n-type region **64**. If it is desired that the impurity concentration in the n-type regions **62**, **62'** differ from that in the n-type region **64**, the n-type regions **62**, **62'** have only to be formed independently from the n-type region **64**, using a specific mask.

FIG. **32** is a detailed sectional view taken along line XIII–XIII' of FIG. **11**.

In the embodiment, to shorten the channel length of the data storage MOS transistor MT, the very thin silicon oxide film **66** is formed on the entire surface of the SDG region overlapping with the floating-gate electrode **71**.

However, if the n-type region **63** is formed of only n-type impurities of a single type, the following drawback will arise:

If the n-type region **63** is formed of only n-type impurities of a single type, the end of the drain region across the channel width of the data storage MOS transistor MT will be positioned directly under the very thin silicon oxide film **66**.

Accordingly, when writing is done by applying a high potential to the drain region **63** of the data storage MOS transistor MT and 0 V to the control gate electrode **75**, a depletion layer at the end of the drain region **63** expands as shown in FIG. **32**, allowing a substrate current Is to flow by band-to-band tunneling at the end of the drain region **63** or at the boundary between the SDG region and the field region.

To overcome this drawback, the n-type region **63** is formed of n-type impurities of more than two types whose diffusion coefficient differs from each other, for example, arsenic (As), whose diffusion coefficient is low, and phosphorus (P), whose diffusion coefficient is high.

In this case, a sectional view taken along line XIII–XIII' of FIG. **11** is given in FIG. **33**.

Specifically, the end of the n-type region **63'** formed of n-type impurities whose diffusion coefficient is high (e.g., phosphorus) is positioned directly under the very thick field oxide film **76**.

With such a structure, since the end of the drain region across the channel width of the data storage MOS transistor MT is positioned directly under the very thick field oxide film **76**, a depletion layer at the end of the drain region (n-type region) **63**, **63'** does not spread much, preventing a substrate current due to band-to-band tunneling from flowing.

Furthermore, in the embodiment, the impurity concentration at the surface necessary for the drain region of the data storage MOS transistor MT is maintained by n-type impurities whose diffusion coefficient is low, and the position of

the end of the drain region is controlled by n-type impurities whose diffusion coefficient is high. Therefore, the write characteristics can be improved by using n-type impurities whose diffusion coefficient is low, and a substrate current can be prevented using n-type impurities whose diffusion coefficient is high.

Forming such a structure out of n-type impurities of a single type whose diffusion coefficient is high (e.g., phosphorus) makes difficult the setting of the impurity concentration at the surface of the drain region, or the control of the position of the drain region's end.

Specifically, an attempt to optimize the impurity concentration at the surface of the drain region permits the drain region to penetrate the channel portion of the data storage MOS transistor, for example. An attempt to limit the extension of the drain region due to diffusion lowers the impurity concentration at the surface of the drain region, resulting in an insufficient write current.

As explained above, the method of manufacturing nonvolatile semiconductor memory devices according to the invention produces the following effects.

Since a very thin silicon oxide film is formed on the drain region and the channel region of the data storage MOS transistor, both the channel length and the channel width can be shortened as compared with those of a conventional equivalent. As a result, the memory cell area can be made smaller.

Furthermore, the drain region of the data storage MOS transistor is composed of an n-type region whose impurity concentration is high, and an n-type region whose impurity concentration is more than several times lower than the high impurity concentration in the preceding n-type region. On the end of the channel length of the n-type region whose impurity concentration is high, there is a slit-like opening and therefore no floating-gate electrode exists above the end.

Additionally, by forming the n-type region whose impurity concentration is high out of impurities whose diffusion coefficient is high and impurities whose diffusion coefficient is low, a field oxide film is located on the end of the channel width.

Consequently, not only can a substrate current in a write operation be prevented, but an internal step-up operation and a low power-consuming operation can also be performed.

Additional advantages and modifications will readily occur to those skilled in the art. Therefore, the invention in its broader aspects is not limited to the specific details, representative devices, and illustrated examples shown and described herein. Accordingly, various modifications may be made without departing from the spirit or scope of the general inventive concept as defined by the appended claims and their equivalents.

What is claimed is:

1. A nonvolatile semiconductor memory device comprising:

a semiconductor substrate with an element region and a field region;

a select MOS transistor formed in said element region; and

a data storage MOS transistor which is formed in said element region and which includes a source region, a drain region, a floating-gate electrode, and a control gate electrode, said floating-gate electrode having a first portion above said drain region and a second portion above said semiconductor substrate between said source region and said drain region, an insulating film thinner than a gate insulating film of said select MOS transistor being arranged between said drain region and said first portion of said floating-gate electrode and between said semiconductor substrate and said second portion of said floating-gate electrode, and said first and second portions of said floating-gate electrode being spaced apart above said element region, and connected to each other on said field region.

2. A nonvolatile semiconductor memory device according to claim **1**, wherein said drain region of said data storage MOS transistor includes:

a first drain region portion arranged in a region including a place directly under said first portion of said floating-gate electrode, and a first side of which is under the space between said first and second portions of said floating-gate electrode; and

a second drain region portion, a first side of which is placed on the side of said second portion of said floating-gate electrode, and a second side of which is connected to said first side of said first drain region portion, said second drain region portion having an impurity concentration which is set at least several times lower than the impurity concentration of said first drain region portion.

3. A nonvolatile semiconductor memory device according to claim **2**, wherein said drain region of said data storage MOS transistor further includes a third drain region portion, a first side of which is connected to the second side of said first region, and a second side of which is placed on the side of a gate electrode of said select MOS transistor.

4. A nonvolatile semiconductor memory device according to claim **3**, wherein the impurity concentration in said second drain region portion is equal to the impurity concentration in said third drain region portion.

5. A nonvolatile semiconductor memory device according to claim **3**, wherein said first, second and third drain region portions also function as a source region of said select MOS transistor.

6. A nonvolatile semiconductor memory device according to claim **5**, wherein the impurity concentration of said first drain region portion and that in said second drain region portion are set so that, when a positive potential is applied to said drain region of said data storage MOS transistor and a ground potential to said control gate electrode, a current starts to flow from said drain region of said data storage MOS transistor to said floating-gate electrode before a current starts to flow from said drain region of said data storage MOS transistor to said semiconductor substrate.

7. A nonvolatile semiconductor memory device according to claim **2**, wherein said first drain region portion includes impurities of more than two types whose diffusion coefficient differs from each other, with the impurities whose diffusion coefficient is lower than the remaining ones of said impurities of more than two types determining the impurity concentration at the surface of said drain region of said data storage MOS transistor, and the impurities whose diffusion coefficient is higher than the remaining ones of said impurities of more than two types extending to directly under said field region.

8. A nonvolatile semiconductor memory device according to claim **7**, wherein said impurities of more than two types whose diffusion coefficient differs from each other contain arsenic and phosphorus.

9. A nonvolatile semiconductor memory device according to claim **1**, wherein said insulating film between said drain region and said first portion of said floating-gate electrode functions as a tunnel insulating film through which Fowler-Nordheim tunneling current flows, and said insulating film between said semiconductor substrate and said second por-

tion of said floating-gate electrode functions as a gate insulating film of said data storage MOS transistor and as a tunnel insulating film.

10. A nonvolatile semiconductor memory device according to claim **1**, wherein said insulating film between said drain region and said first portion of said floating-gate electrode and that between said semiconductor substrate and said second portion of said floating-gate electrode has a thickness of approximately 10 nm, and the gate insulating film of said select MOS transistor has a thickness of several tens nm.

11. A nonvolatile semiconductor memory device according to claim **1**, wherein in said element region, the shape of said control gate electrode is the same as that of said floating-gate electrode.

12. A semiconductor memory device including a memory cell having a selection transistor and a data storage transistor, comprising:

a semiconductor substrate of a first conductivity type;

a field insulating film formed on said semiconductor substrate to define an element region;

first, second, and third impurity regions of a second conductivity type formed in said element region of said semiconductor substrate;

a gate electrode of said selection transistor provided above a first channel region between said first and second impurity regions;

a floating gate electrode of said data storage transistor having a first electrode portion provided over at least a portion of said second impurity region, and a second electrode portion, spaced apart from said first electrode portion, provided over a second channel region between said second impurity region and said third impurity region;

a first insulating film formed between said first electrode portion of said floating gate electrode and said at least a portion of said second impurity region and between said second electrode portion of said floating gate electrode and said second channel region; and

a second insulating film formed between said gate electrode of said selection transistor and said first channel region,

wherein the thickness of said first insulating film is less than the thickness of said second insulating film.

13. A semiconductor memory device according to claim **12**, wherein the thickness of said first insulating film is approximately 10 nanometers and the thickness of said second insulating film is approximately several tens of nanometers.

14. A semiconductor memory device according to claim **12**, wherein said second impurity region includes a first impurity region portion arranged between second and third impurity region portions.

15. A semiconductor memory device according to claim **14**, wherein a junction between said first impurity region portion and said second impurity region portion is below the space between said first and second electrode portions of said floating gate electrode.

16. A semiconductor memory device according to claim **15**, wherein a junction between said second impurity region portion and said semiconductor substrate is below an edge of the second electrode portion of said floating gate electrode.

17. A semiconductor memory device according to claim **15**, wherein the impurity concentration of said second impurity region portion is less than the impurity concentration of said first impurity region portion.

18. A semiconductor memory device according to claim **17**, wherein the impurity concentration of said third impurity region portion is approximately the same as the impurity concentration of said second impurity region portion.

19. A semiconductor memory device including a memory cell having a selection transistor and a data storage transistor, comprising:

a semiconductor substrate of a first conductivity type;

a field insulating film formed on said semiconductor substrate to define an element region;

first, second, and third impurity regions of a second conductivity type formed in said element region of said semiconductor substrate;

a gate electrode of said selection transistor provided above a first channel region between said first and second impurity regions;

a floating gate electrode of said data storage transistor having a first electrode portion provided at least partly over a first portion of said second impurity region having a first impurity concentration and a second electrode portion provided over a second channel region between a second portion of said second impurity region having a second impurity concentration and said third impurity region.

20. The semiconductor memory device according to claim **19**, wherein said second impurity region includes a third portion having a third impurity concentration such that said first portion of said second impurity region is disposed between said second and third portions of said second impurity region.

21. The semiconductor memory device according to claim **20**, wherein the second and third impurity concentrations are approximately equal.

22. The semiconductor memory device according to claim **21**, wherein the first impurity concentration is greater than the second and third impurity concentrations.

23. The semiconductor memory device according to claim **19**, wherein said second impurity region constitutes a drain of said data storage transistor and a source of said selection transistor.

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